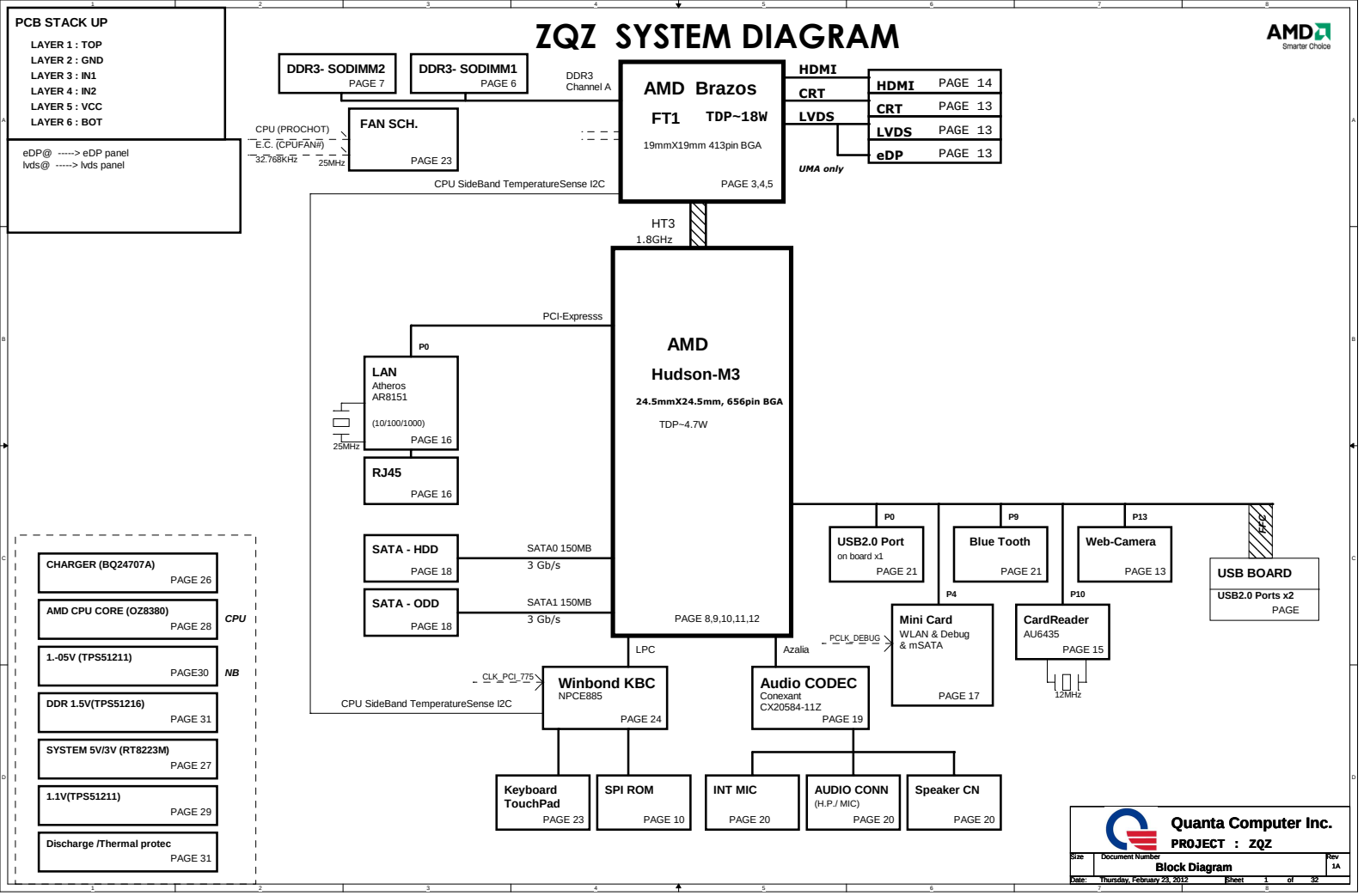
ZQZ SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

eDP@ -----> eDP panel
lvds@ -----> lvds panel



CPU

- CHARGER (BQ24707A) PAGE 26
- AMD CPU CORE (OZ8380) PAGE 28
- 1.-05V (TPS51211) PAGE30

NB

- DDR 1.5V(TPS51216) PAGE 31
- SYSTEM 5V/3V (RT8223M) PAGE 27
- 1.1V(TPS51211) PAGE 29
- Discharge /Thermal protec PAGE 31

Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	Block Diagram	1A

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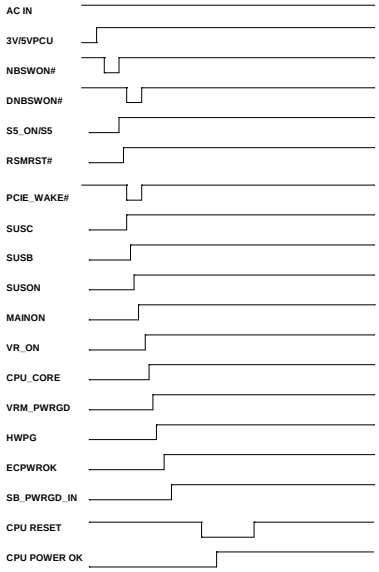
INDEX

Power Sequence



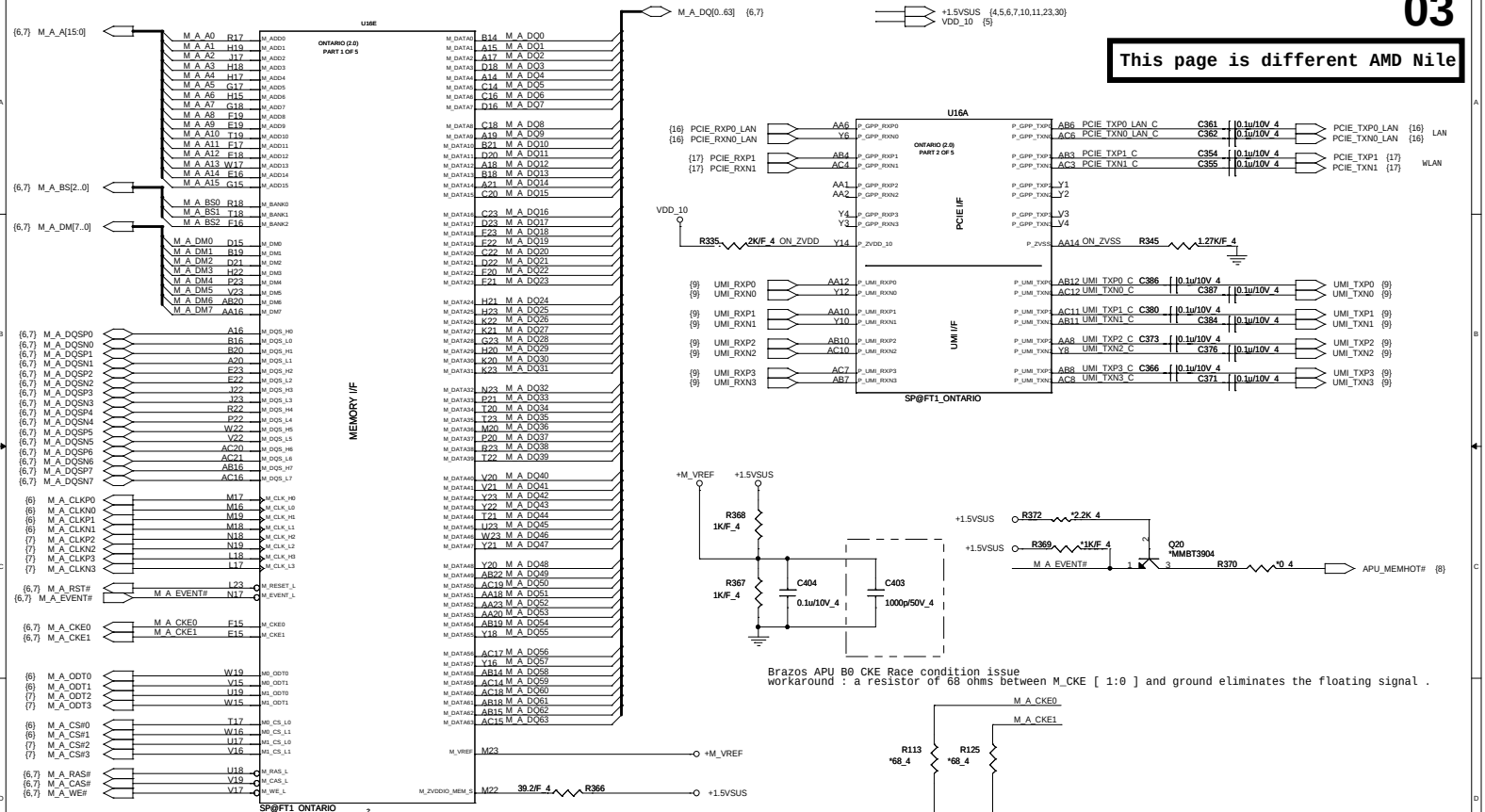
Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

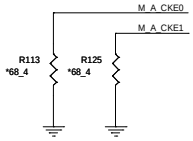
KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nile



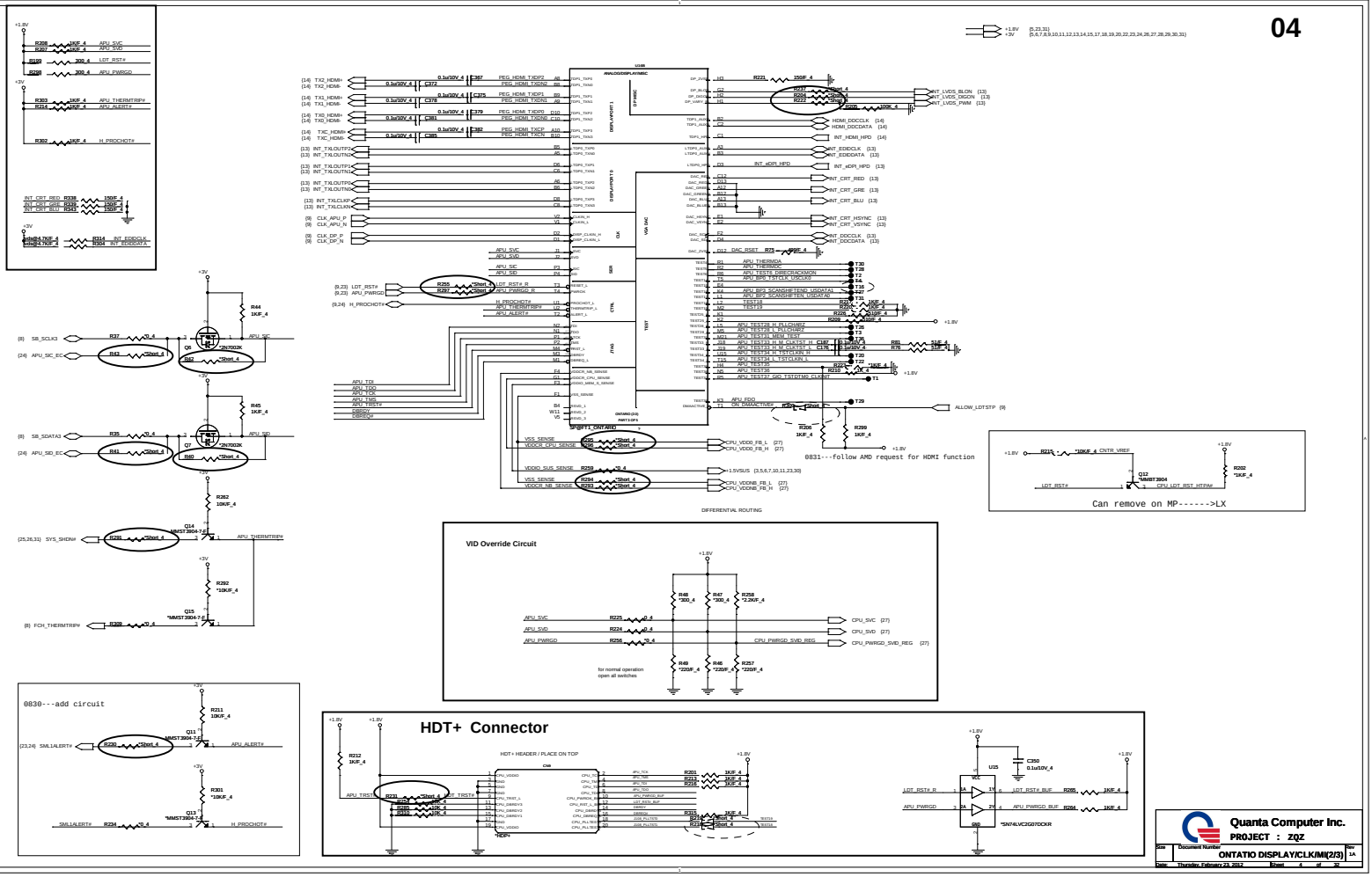
Brazos APU B0 CKE Race condition issue
workaround : a resistor of 68 ohms between M_CKE [1:0] and ground eliminates the floating signal .



P/N	Item Description
AJ01200TT00	CPU(413P)EM1200GBB22GV 1.4G(BGA)
AJ01200TT01	CPU(413P)EM1200GBB22GV 1.4G(BGA)STN BSQ
AJ01800VT00	CPU(413P)EM1800GBB22GV 1.7G(BGA)
AJ01800VT01	CPU(413P)EM1800GBB22GV 1.7G(BGA)STN BSQ

Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	ONTARIO MEM & PCIE I/F(1/3)	1A
Date: Thursday, February 23, 2012	Sheet 3 of 32	


0831---follow AMD request for HDMI function
DIFFERENTIAL ROUTING
Can remove on MP------>LX
VID Override Circuit
for normal operation
open all switches
0830---add circuit
HDT+ Connector
HDT+ HEADER / PLACE ON TOP
Quanta Computer Inc.
PROJECT : ZQZ
ONTATIO DISPLAY/CLK/MI(2/3)
Thursday, February 23, 2012

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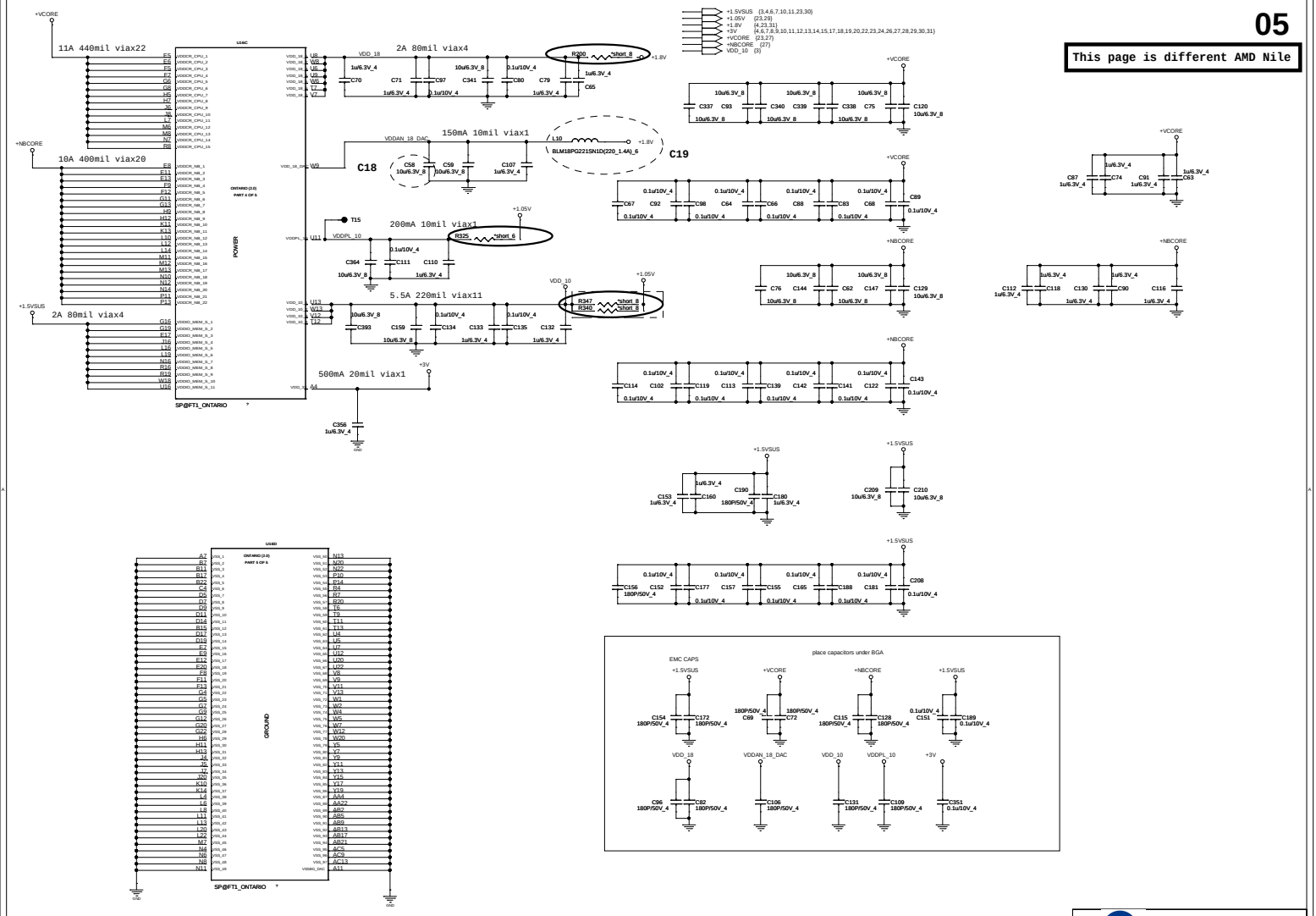


Quanta Computer Inc.			
PROJECT : ZQZ			
Size	Document Number		Rev
	ONTARIO POWER & DECOUP(3/3)		1A
Date: Thursday, February 23, 2012		Sheet 5 of 32	

0830--P/N and footprint are follow ZR7B

+1.5VSUS (3,4,5,7,10,11,23,30)
+0.75V_DDR_VTT (7,30)
+3V (4,5,7,8,9,10,11,12,13,14,15,17,18,19,20,22,23,24,26,27,28,29,30,31)

CN15A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=9.2_STD

BUS1_A2

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

CN15B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=9.2_STD

600mA

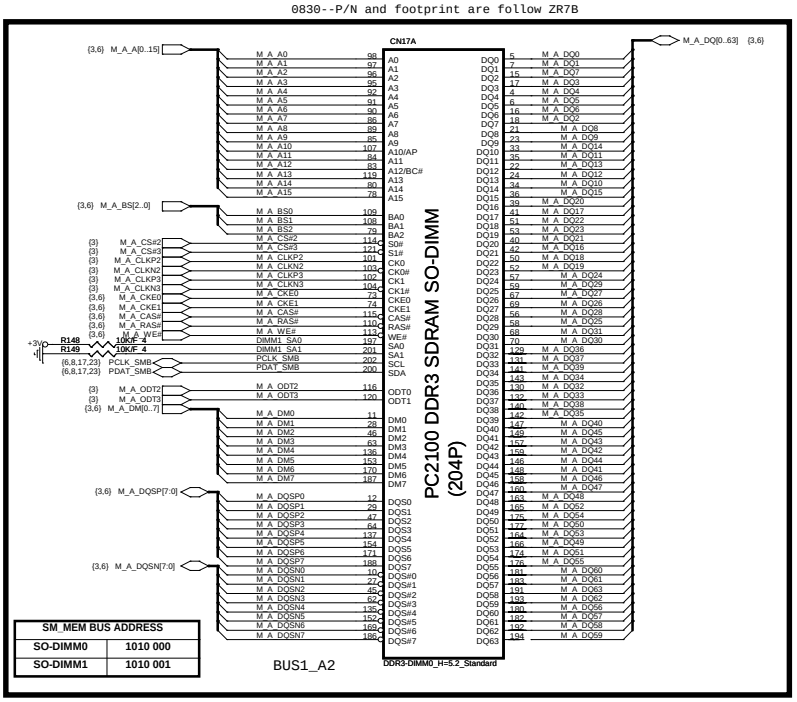
3mA

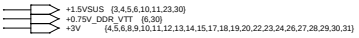
+SMDDR_VREF

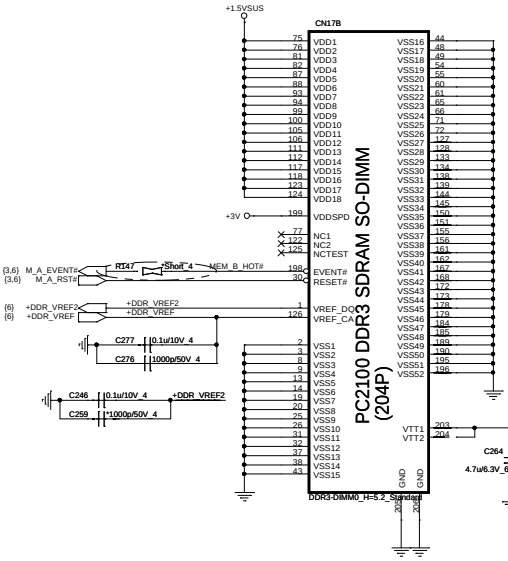
Quanta Computer Inc.
PROJECT : ZQZ

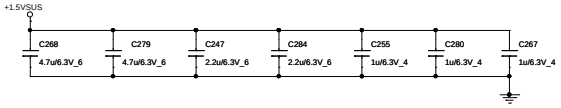
Size	Document Number	Rev
	DDR3 SO-DIMM (STD)	1A
Date: Thursday, February 23, 2012	Sheet 6 of 32	

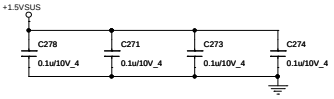
0830--P/N and footprint are follow ZR7B

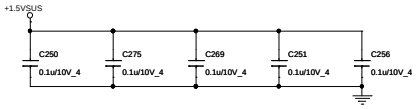


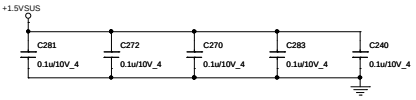


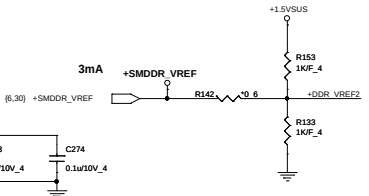












Quanta Computer Inc.	
PROJECT : ZQZ	
Size	Document Number: DDR3 SO-DIMM (STD) — Rev: 1A
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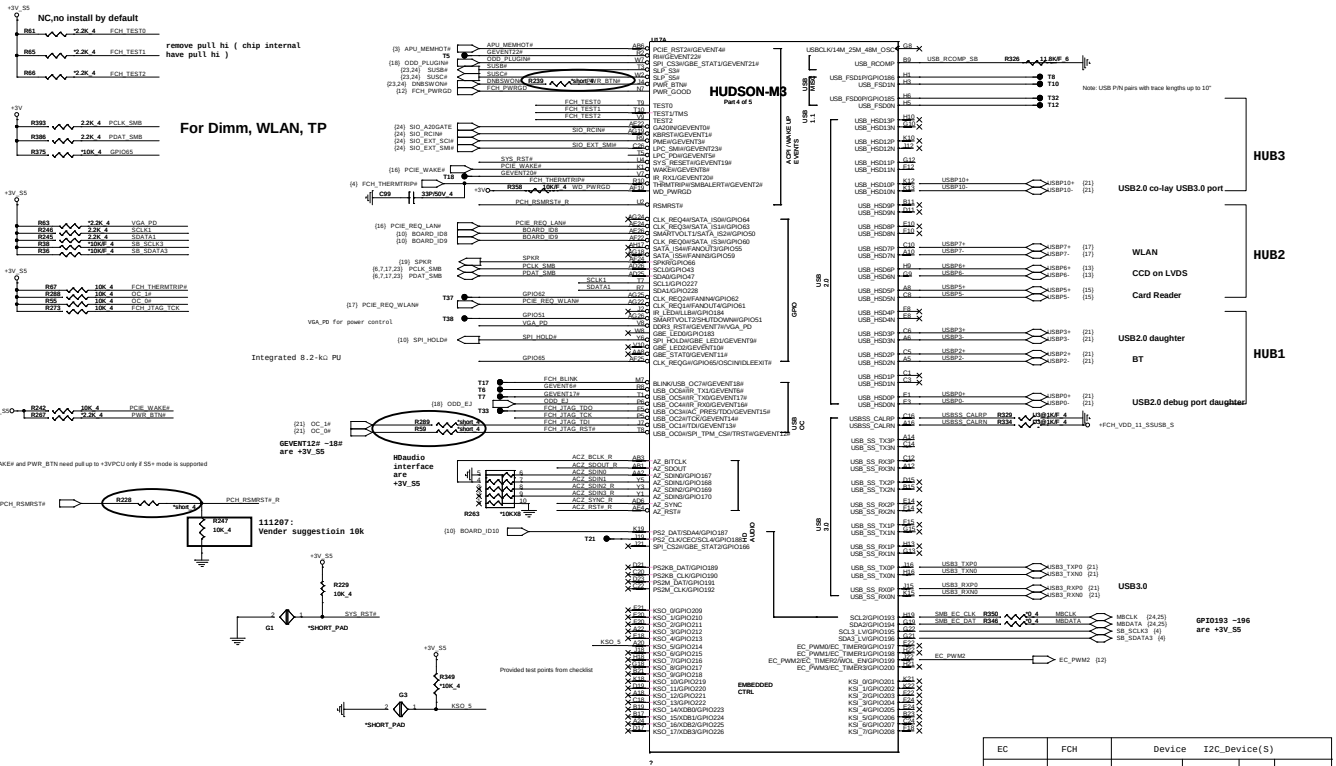
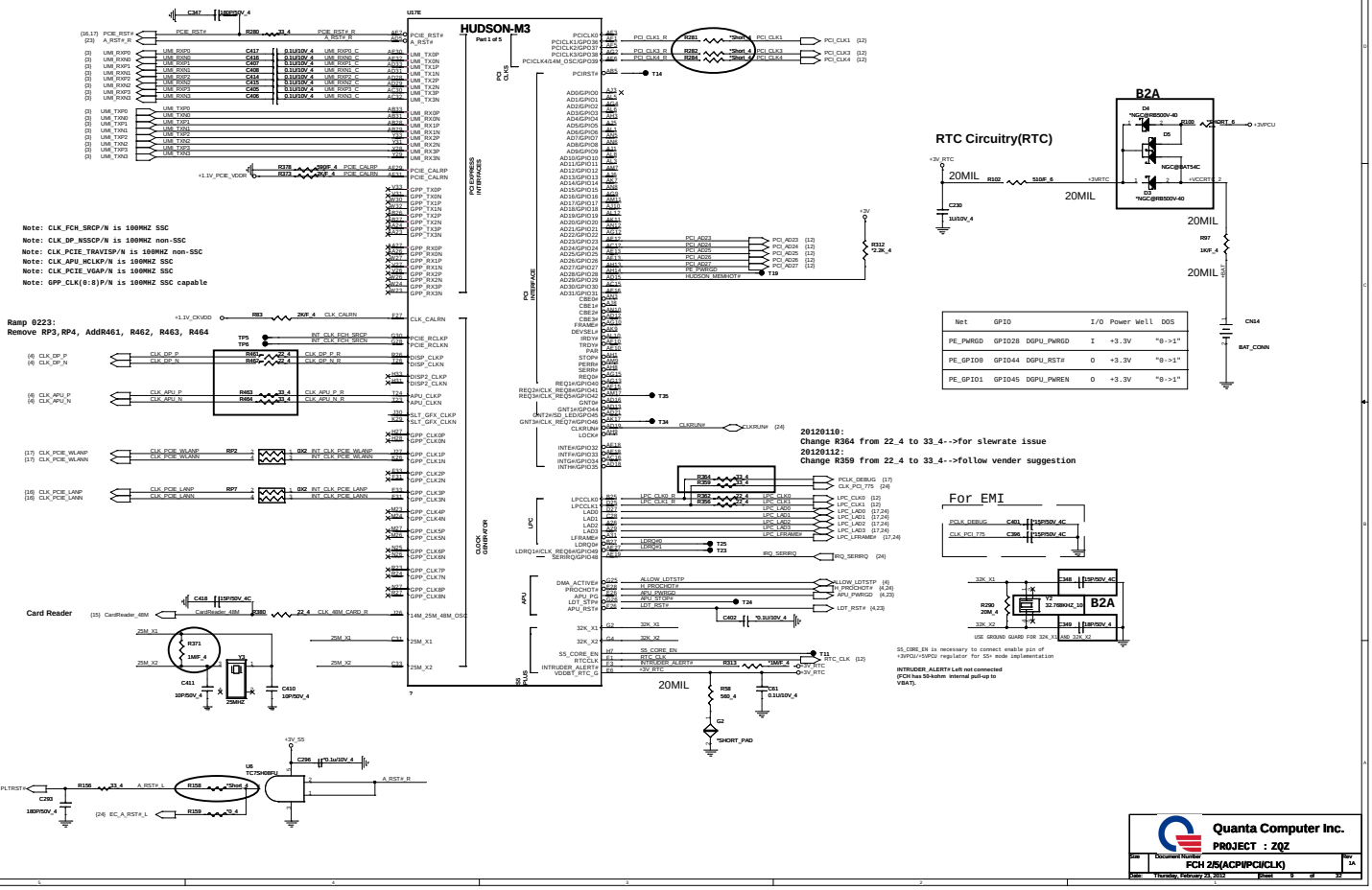


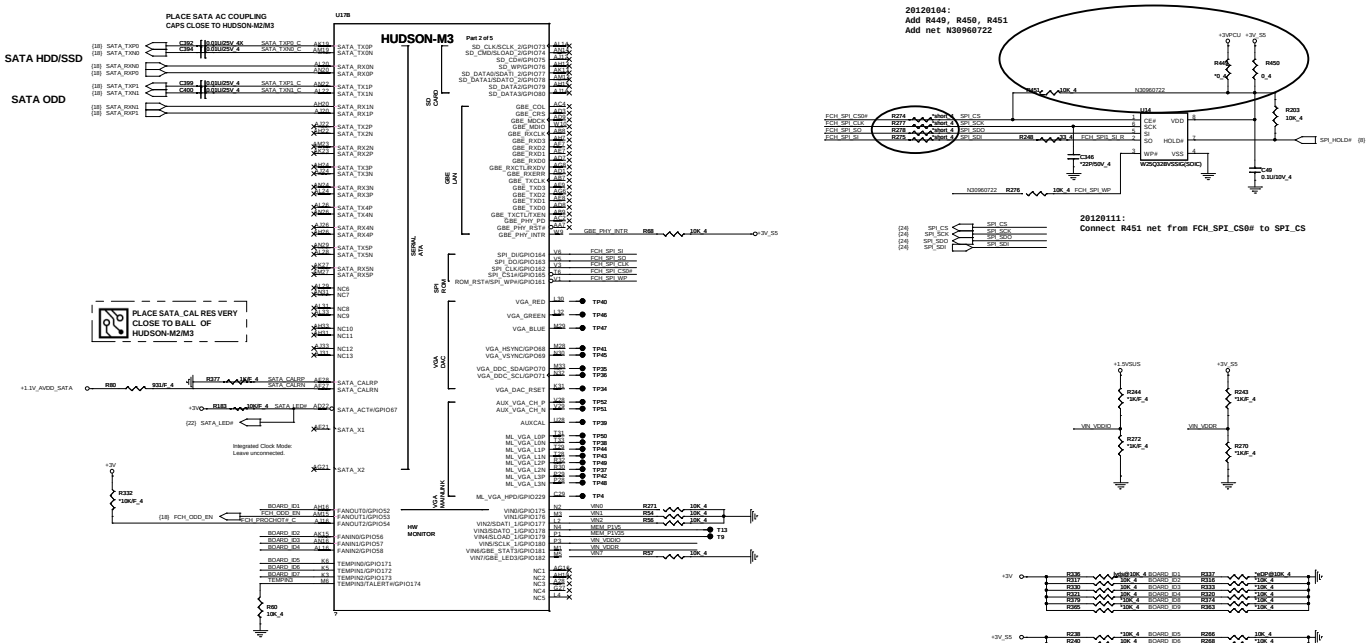
EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		EEPROM	APU		ALL
I2Ce_3(M)		VGA Thermal			
	I2Cf_3(M)			APU	S5
	I2Cf_1(M)	Lan	WLan		S5
	I2Cf_0(M)	Dimm	Clk Gen		S0

EC will Conflict with FCH, did not mount R3154&R318

Quanta Computer Inc.
PROJECT : ZQZ
Size | Document Number | Rev 1A
FCH 1/5(GPIO/USB/AZ)
Date: Thursday, February 23, 2012 | Sheet 8 of 32



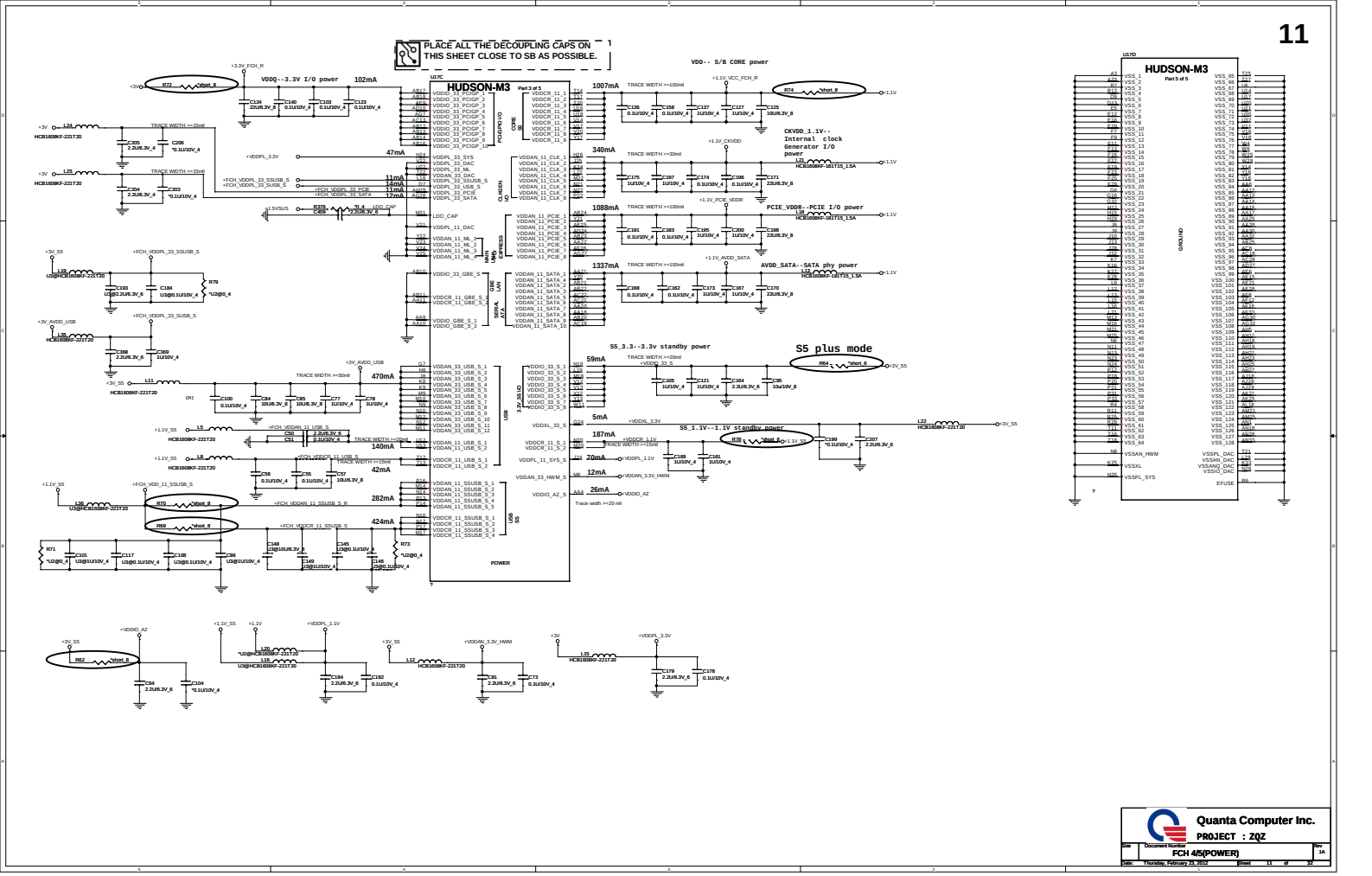
Quanta Computer Inc.
PROJECT : ZQZ
Size: Document Number: FCH 2/5(ACPI/PCI/CLK) Rev: 1A
Date: Thursday, February 23, 2012 Sheet 9 of 32



BOARD_ID1	LCD
0	eDP
1	LVDS

BOARD_ID2	BOARD_ID3	For TP
0	1	ALPS
1	0	ELAN
1	1	Synaptics

Quanta Computer Inc.			
PROJECT : ZQZ			
Size	Document Number		Rev
	FCH 3/5(SATA/VGA/GND/SPI)		1A
Date: Thursday, February 23, 2012	Sheet 10 of 32		


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
VDDQ--3.3V I/O power
102mA
HUDSON-M3
Part 3 of 5
VDD-- S/B CORE power
1007mA
CKVDD_1.1V--Internal clock Generator I/O power
340mA
PCIE_VDDR--PCIE I/O power
1088mA
AVDD_SATA--SATA phy power
1337mA
S5_3.3--3.3v standby power
59mA
S5 plus mode
S5_1.1V--1.1V standby power
187mA
5mA
HUDSON-M3
Part 5 of 5
Quanta Computer Inc.
PROJECT : ZQZ
FCH 4/5(POWER)
Rev 1A
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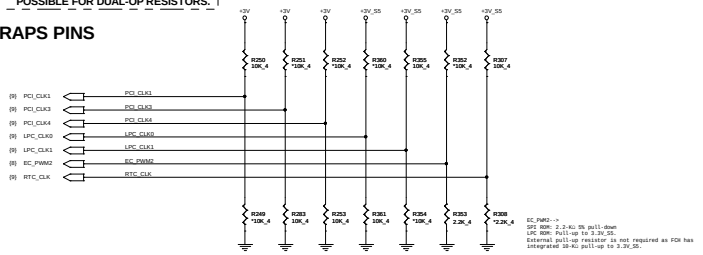
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

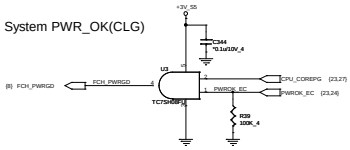


Remove PCI_CLK2 function

REQUIRED STRAPS

	*********	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	*********	ALLOW PCIE Gen2 DEFAULT	*********	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*********	FORCE PCIE Gen1	*********	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

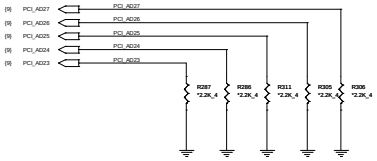
System PWR_OK(CLG)



FCH PWRGD CKT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : ZQZ
Size | Document Number | Rev
FCH 5/5(STRAP & PWRGD) | 1A
Date: Thursday, February 23, 2012 | Sheet 12 of 32

CRT

OPTION SIGNAL FROM NB to LVDS/CRT for UMA

{4} INT_DDCCLK — INT_DDCCLK
{4} INT_DDCDATA — INT_DDCDATA
{4} INT_CRT_HSYNC — INT_CRT_HSYNC
{4} INT_CRT_VSYNC — INT_CRT_VSYNC
{4} INT_CRT_RED — INT_CRT_RED
{4} INT_CRT_GRE — INT_CRT_GRE
{4} INT_CRT_BLU — INT_CRT_BLU

30V/ 1A
30V/ 0.5A

+5V — F1 SMD1206P100TF — CRTVDD5_F — D15 B0520WS-7-F — CRTVDD5
C126 22u/10V_4

INT_CRT_RED — L23 BLM18BB750SN1D — CRT_R1
INT_CRT_GRE — L17 BLM18BB750SN1D — CRT_G1
INT_CRT_BLU — L14 BLM18BB750SN1D — CRT_B1

R84 150/F_4, R82 150/F_4, R77 150/F_4
C202 10P/50V_4, C186 10P/50V_4, C163 10P/50V_4
C166 10P/50V_4, C185 10P/50V_4, C201 10P/50V_4

CN11 CRT
CRT_R1, CRT_G1, CRT_B1, CRT_11, DDCDAT_1, CRTHSYNC, CRTVSYNC, DDCCLK_1
TP33

20120110:
Change L14, L17, L23 from BLM18BA470SN1_6 to BLM18BB750SN1D

+3V — C397 0.1u/10V_4 — C388 22u/10V_4 CRT_BYP — C391 0.1u/10_V_4

U18 CM2009-02QR
CRTVDD5 — VCC_SYNC, VCC_DDC, VCC_VIDEO, GND
SYNC_OUT2 — CRTVSYNC
SYNC_OUT1 — CRTHSYNC
BYP
SYNC_IN2 — INT_CRT_VSYNC
SYNC_IN1 — INT_CRT_HSYNC
CRT_R1 — VIDEO_1
CRT_G1 — VIDEO_2
CRT_B1 — VIDEO_3
DDC_IN1 — INT_DDCCLK
DDC_IN2 — INT_DDCDATA
DDC_OUT1 — DDCCLK_1
DDC_OUT2 — DDCDAT_1

+3V — R348 2.7K_4, R351 2.7K_4
R344 2.7K_4, R357 2.7K_4 — CRTVDD5

C398 1000p/50V, C389 10P/50V_4, C390 10P/50V_4, C383 10P/50V_4, C395 10P/50V_4

20120110:
Change C398 from .1u_10V_4 to 1000p/50V_4

LVDS(LDS)

+3V — C18 10P/50V_4 — C17 1000P/50V_4
VIN — C16 4.7u/25V_8 — C6 1000P/50V_4
+3V — L2 *short_6 — C20 *0.1u/10V_4 — LCD_POWER — C8 *10P/50V_4
VIN — L1 *short_6, L4 *short_6, C12 *10P/50V_4, C11 *10P/50V_4 — LCD_VIN

20120104:
Swap INT_EDIDCLK from CN1.32 to CN1.33
Swap INT_EDIDDATA from CN1.33 to CN1.32

CN1

LCD_VIN
R15 *eDP@100K_4, R16 *eDP@100K_4
{4} INT_EDIDCLK — INT_EDIDCLK — C14 *eDP@0.1u/10V_4
{4} INT_EDIDDATA — INT_EDIDDATA — C15 *eDP@0.1u/10V_4
{4} INT_TXLOUTP2 — INT_TXLOUTP2 — C10 *eDP@0.1u/10V_4 — eDP_MLP0
{4} INT_TXLOUTN2 — INT_TXLOUTN2 — C9 *eDP@0.1u/10V_4 — eDP_MLN0
EDP_EDIDCLK
EDP_EDIDDATA
{4} INT_TXLCLKP — INT_TXLCLKP
{4} INT_TXLCLKN — INT_TXLCLKN
{4} INT_TXLOUTP0 — INT_TXLOUTP0
{4} INT_TXLOUTN0 — INT_TXLOUTN0
{4} INT_TXLOUTP1 — INT_TXLOUTP1
{4} INT_TXLOUTN1 — INT_TXLOUTN1
INT_TXLOUTP2 — R25 lvds@0_4 — INT_TXLOUTP2_R
INT_TXLOUTN2 — R24 lvds@0_4 — INT_TXLOUTN2_R
INT_EDIDDATA — R14 lvds@0_4 — LVDS_EDIDDATA
INT_EDIDCLK — R13 lvds@0_4 — LVDS_EDIDCLK
eDP-HPD
{24} CONTRAST
{4} INT_LVDS_PWM
R10 *0_4, R20 short_4 — LVDS_BRIGHT — R12 BLM15AG121SS1/0.5A/120ohm_4
BL_ON
+3V — R17 short_6 — LCDVCC
CCD_POWER
*15P/50V_4C — C21 — R29 *300_4
{8} USBP6- — R19 0_4 — USBP6- R
{8} USBP6+ — R18 0_4 — USBP6+ R
{19} MIC2_INTL1
CCD-USB
ADOGND
GS12401-1011-40P-R-NH

Ramp 0221:
Remove L3

20120104:
R30, R28, Q2, Q3 unstuff, R21 stuff

INT_eDPI_HPD — R21 *short — eDP-HPD
+3V — R30 *10K_4
+3V — R26 *100K_4
{4} INT_eDPI_HPD
Q2 *2N7002K
Q3 *2N7002K
eDP-HPD_R — R28 *0_4 — eDP-HPD
R31 100K_4

LCD PW(LDS)

+3V — C22 1U/6.3V_4
U1 IC(5P) G5243T11U
IN, IN, ON/OFF — OUT, GND, GND
{4} INT_LVDS_DIGON
R31 100K_4
40mil
LCDVCC
C7 1U/6.3V_4, C322 *.1u/10V_4, C323 .01u/16V_4, C19 22u/6.3V_8

LCDVCC — L32 *short — LCDVCC_L
C13 *10P/50V_4, C324 *10P/50V_4

Backlight Control(LDS)

+3VPCU — R9 *100K
+3V — R23 10K_4, R22 10K_4
BL_ON — D2 BAS316 — LID591# {24}
BL# — Q4 2N7002K — Q1 DTC144EUA — EC_FPBACK# {24}
{4} INT_LVDS_BLON — Q5 2N7002K
R27 100K_4

Lid Switch (HSR)

+3VPCU — C4 0.1u/10V_4
HE1 APX9132H AI — LID591#
D1 *VPORT_6

EM-6781-T3: AL006781000
APX9132H AI-TRG: AL009132001
AH9249NTR-G1: AL009249000

Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	CRT/LVDS/LID	1A
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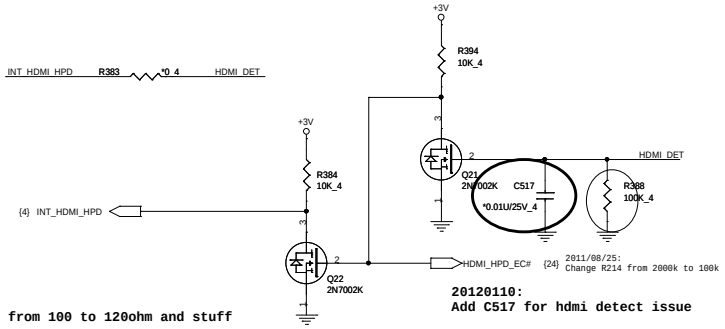
HDMI SDVO I2C Control

{4} HDMI_DDCDATA
{4} HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DDCCLK

HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

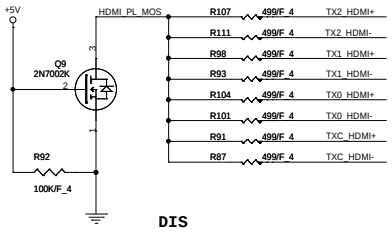


20120110:
Add C517 for hdmi detect issue

HDMI (HDM)

Ramp 0223:
Change R88, R94, R103, R109 value from 100 to 120ohm and stuff

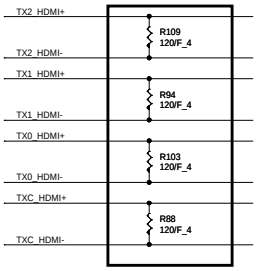
Close to HDMI Connector



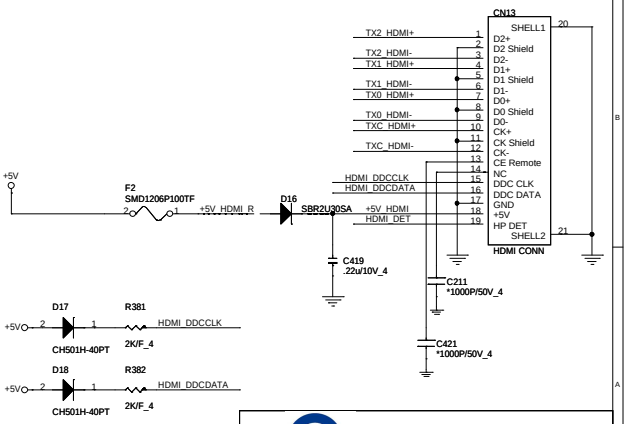
DIS
Stuff 499 ohm CS14992FB24

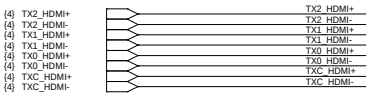
EMI reserve for HDMI(EMC)

Close connector



HDMI PORT (HDM)





Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	HDMI	1A
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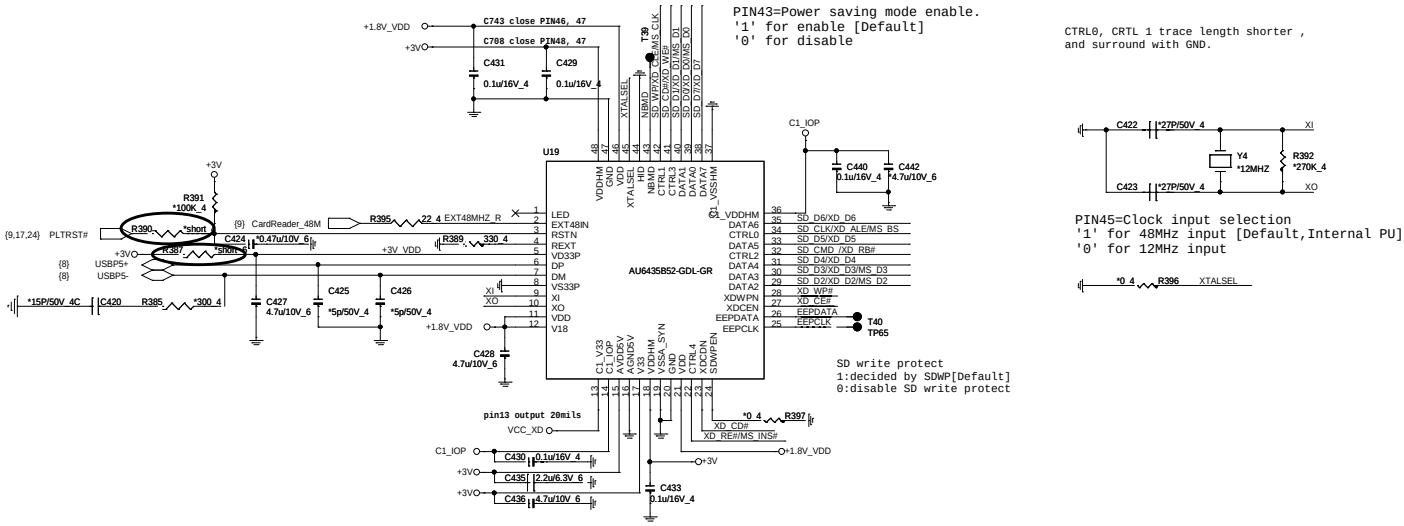
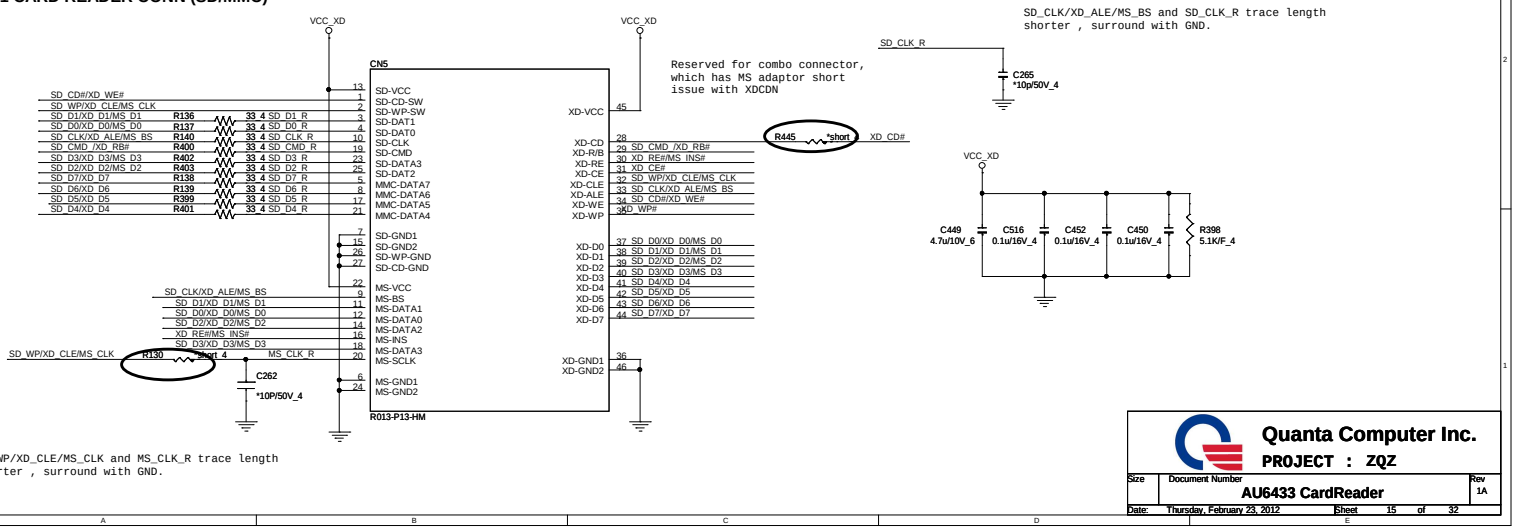
5 in 1 CARD READER IC (SD,MMC,xD,MS)



5 IN 1 CARD READER CONN (SD/MMC)



Quanta Computer Inc.	
PROJECT : ZQZ	
Size	Document Number: AU6433 CardReader — Rev: 1A
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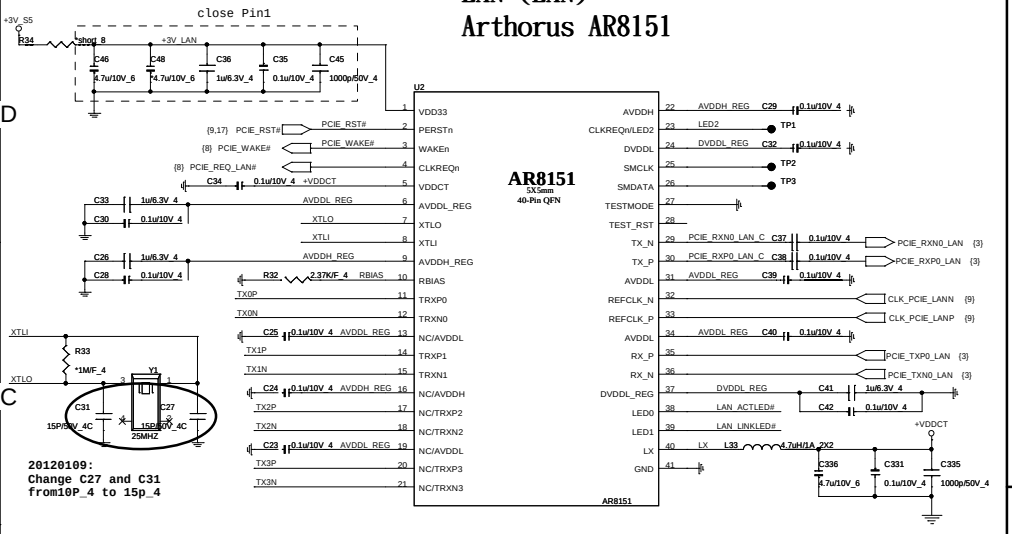
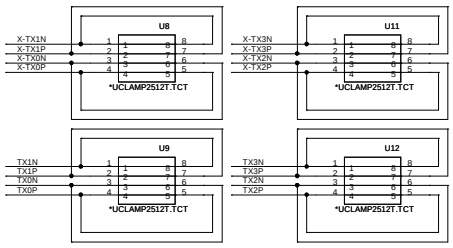
LAN (LAN)
Arthorus AR8151

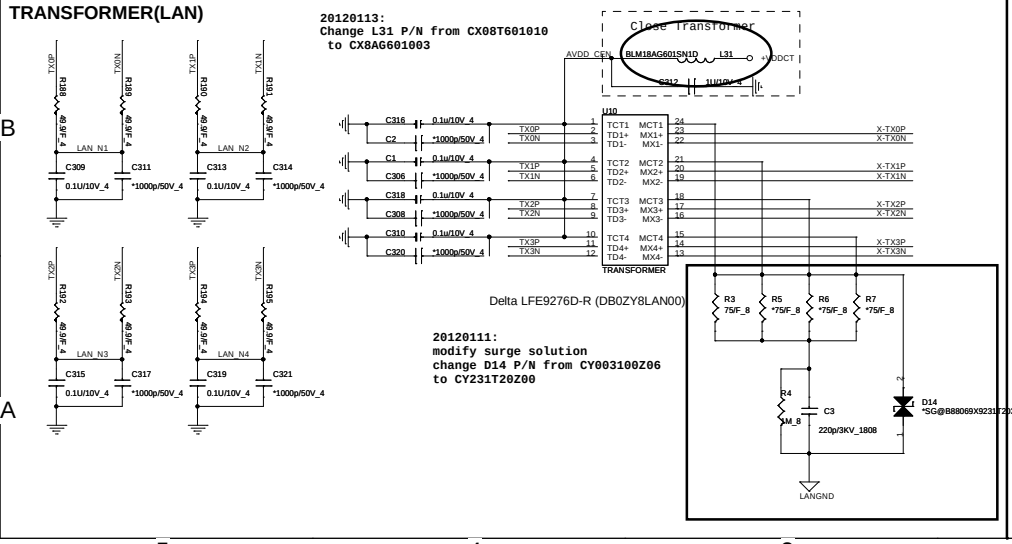


20120109:
Change C27 and C31
from10P_4 to 15p_4



16

TRANSFORMER(LAN)

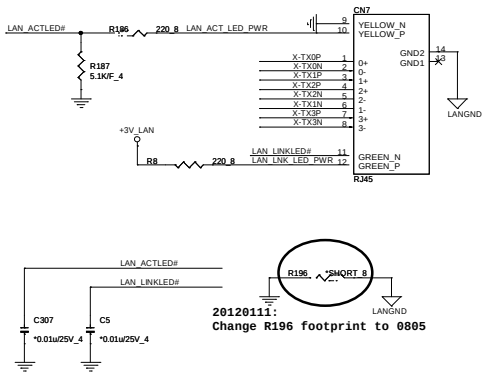


20120113:
Change L31 P/N from CX08T601010
to CX8AG601003

Delta LFE9276D-R (DB0ZY8LAN00)

20120111:
modify surge solution
change D14 P/N from CY003100Z06
to CY231T20Z00

RJ45(LAN)



20120111:
Change R196 footprint to 0805

Quanta Computer Inc.		
PROJECT : ZQZ		
Size	Document Number	Rev
	LAN (AR8151)	1A
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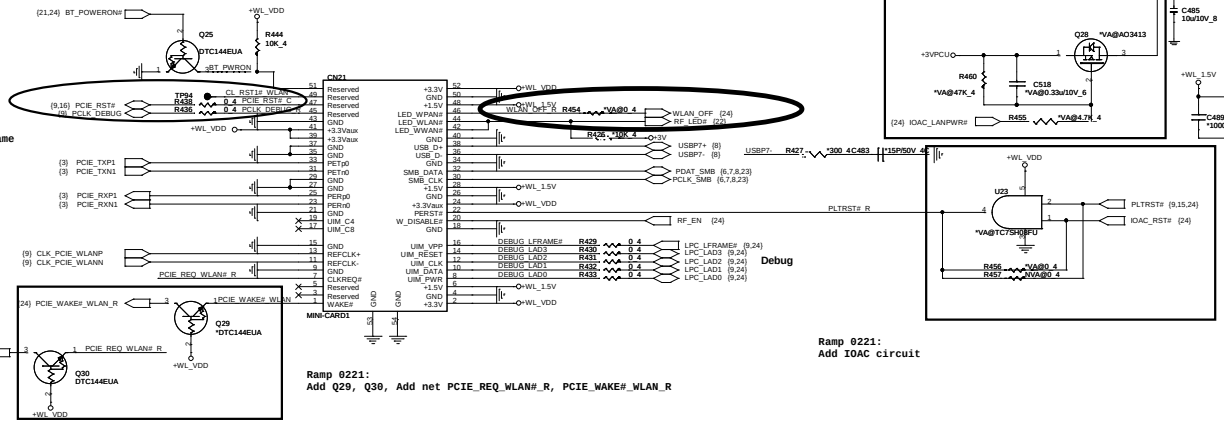
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Ramp 0221:
modify net name

Ramp 0221:
Add Q29, Q30, Add net PCIE_REQ_WLAN#_R, PCIE_WAKE#_WLAN_R

Ramp 0221:
Add IOAC circuit

mSATA

Quanta Computer Inc.		
PROJECT : ZQZ		
Size	Document Number: MINI PCI-E card	Rev 1A
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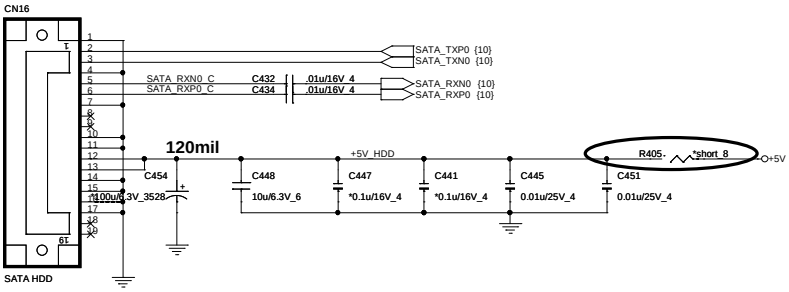
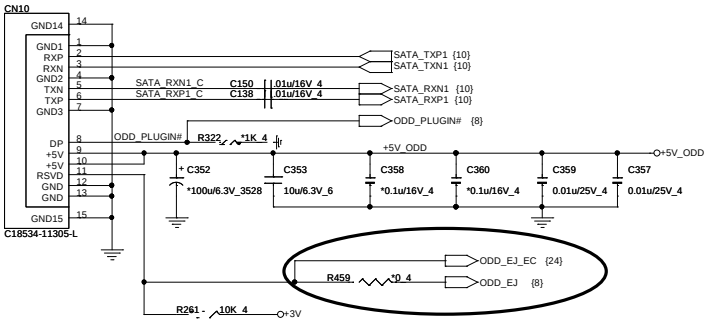
SATA HDD

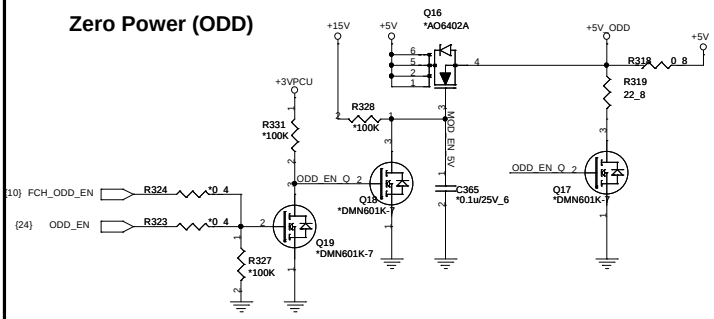


SATA ODD



Ramp 0221:
Add R459

Zero Power (ODD)



Quanta Computer Inc.		
PROJECT : ZQZ		
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
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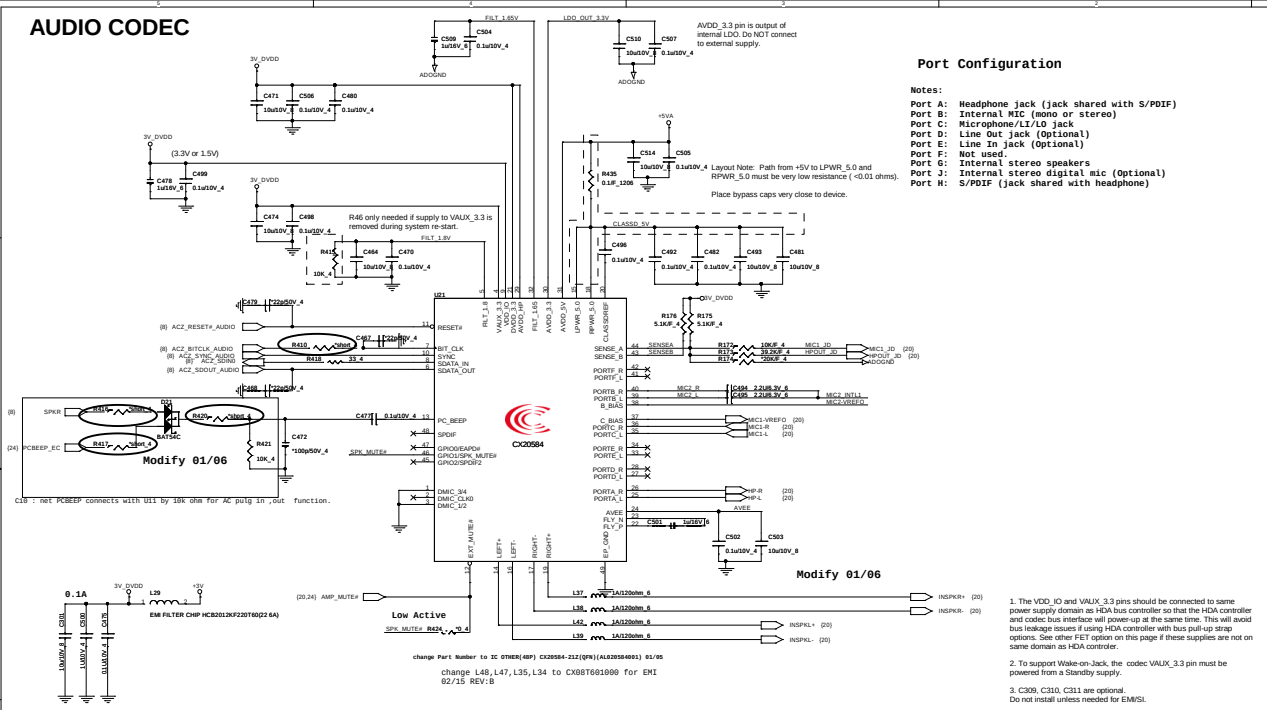
AUDIO CODEC



Port Configuration

Notes:

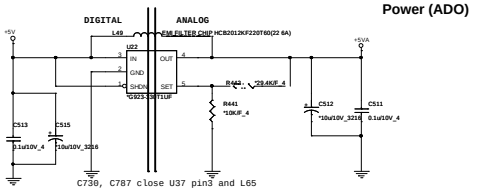
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

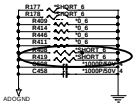
1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controler.

2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.

3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.

Power (ADO)

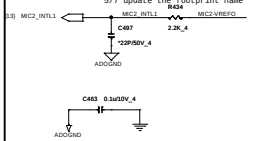




Tied at one point only under the codec or near the codec

INT MIC array

5/7 update the footprint name



cap place close to MIC-connector

Quanta Computer Inc.
PROJECT : ZQZ
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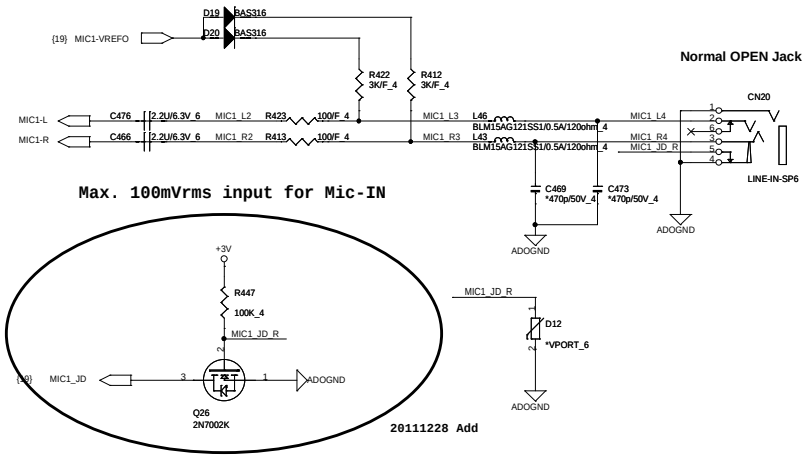
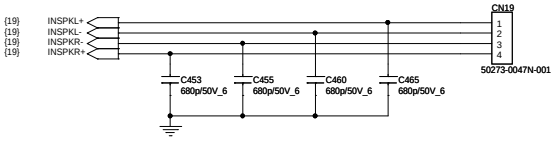
MIC



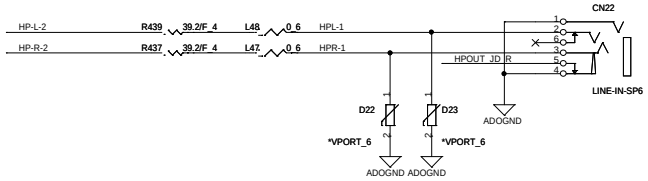
Max. 100mVrms input for Mic-IN

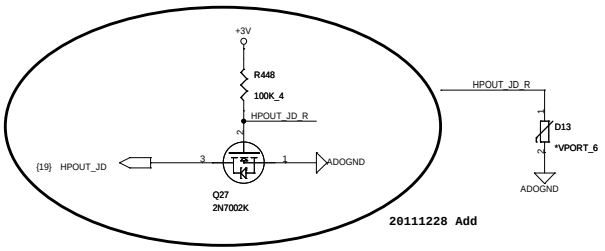
20111228 Add

Internal Speaker

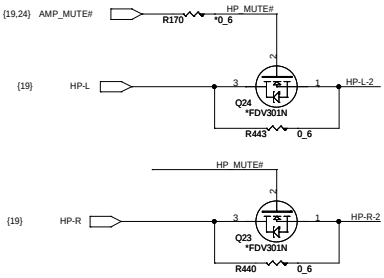


HP





20111228 Add



Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	AUDIO JACK CONN	1A
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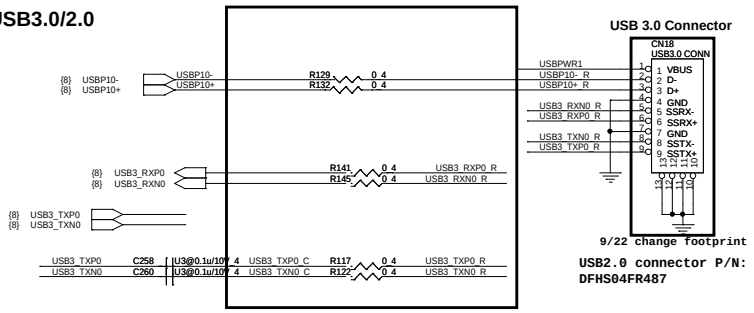
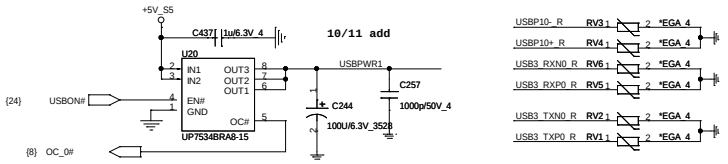
USB3.0/2.0

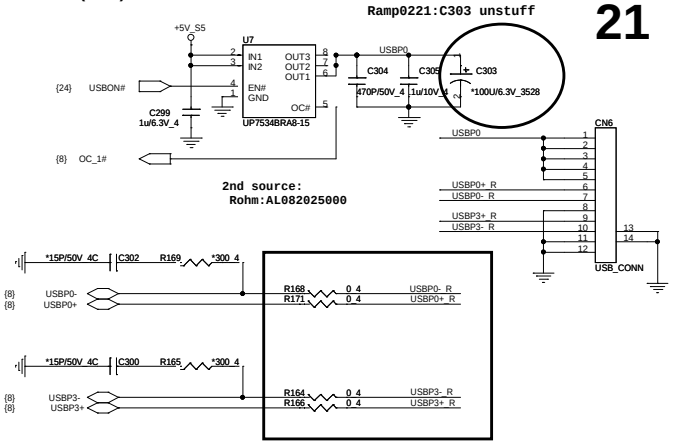


1st source: AL007534000
2ns source: AL082025000



EXT. USB(USB)

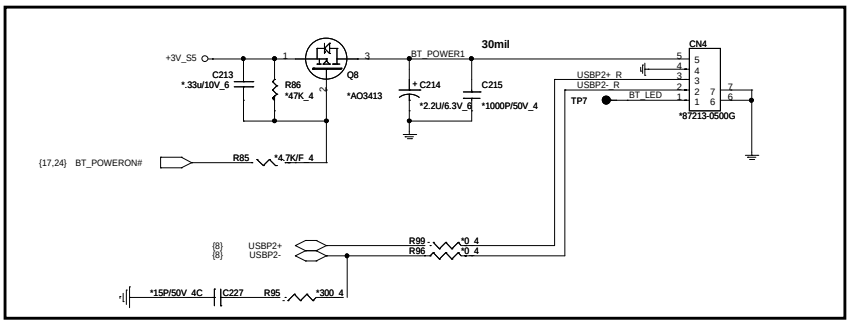
Ramp0221:C303 unstuff



2nd source:
Rohm:AL082025000

BLUETOOTH V3.0 CONN(BTM)

Ramp 0221:
L27, RP5, RP6, L26, L30, L28



Quanta Computer Inc. PROJECT : ZQZ			
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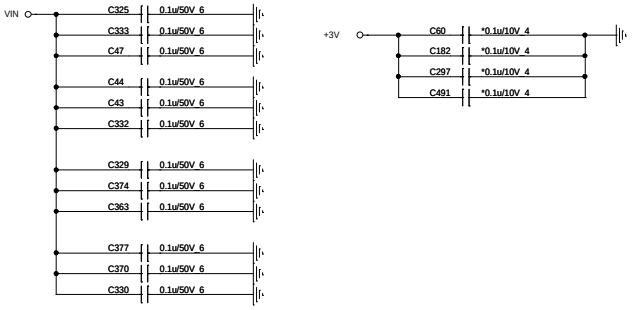
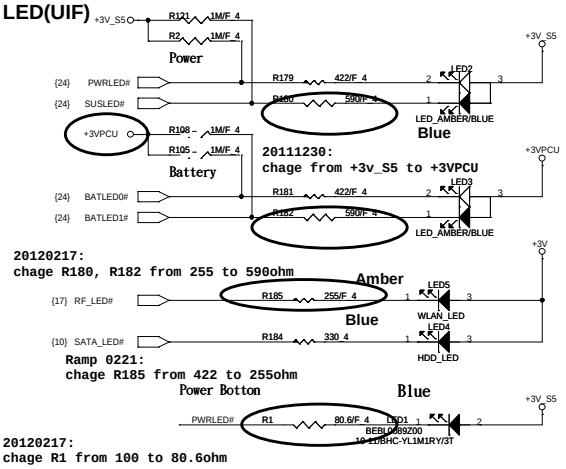
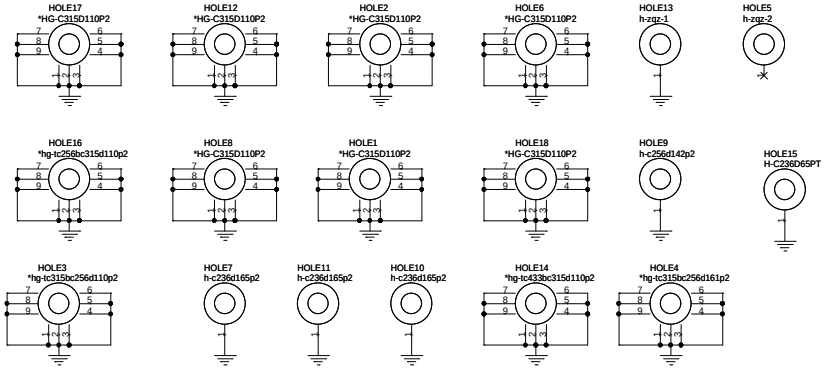
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



HOLE(OTH)



Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	29 -- LED/ EMI/ Screw Hole& Nut	1A
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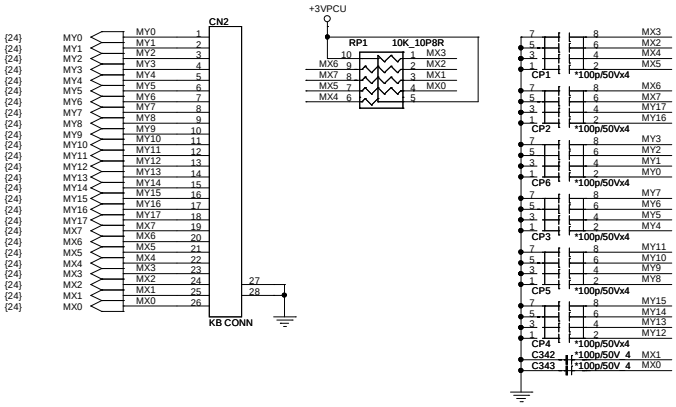
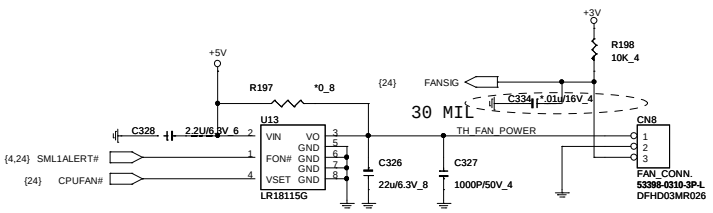
K/B(KBC)

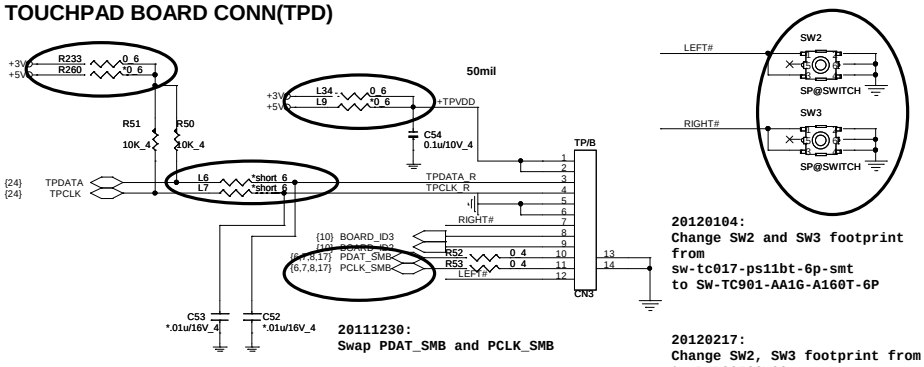


CPU FAN(THM)



23

TOUCHPAD BOARD CONN(TPD)



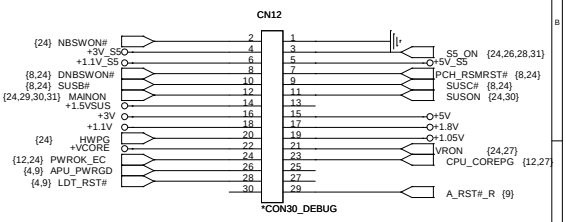
20111230:
Swap PDAT_SMB and PCLK_SMB

20120104:
Change SW2 and SW3 footprint from
sw-tc017-ps11bt-6p-smt
to SW-TC901-AA1G-A160T-6P

20120217:
Change SW2, SW3 footprint from DHP00AC1G01
to DHP00532W00

Power Sequence

0903--Add Connecotr



Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	30 -- KB/TP/FAN	1A
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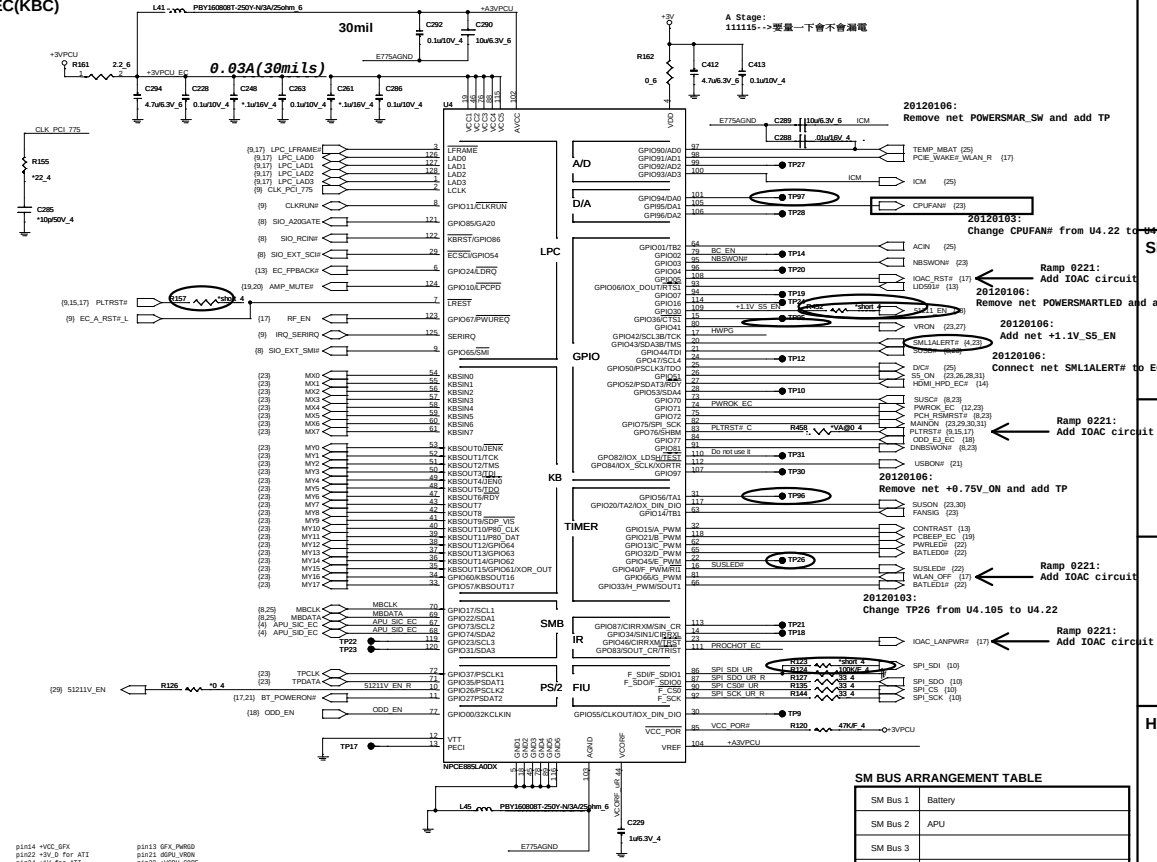
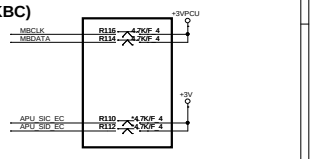
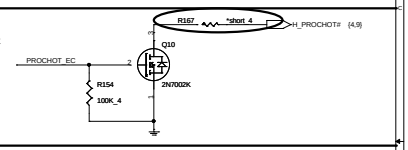
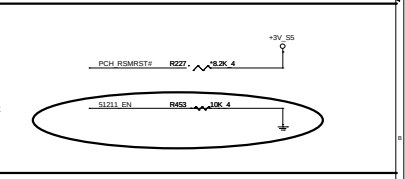
EC(KBC)



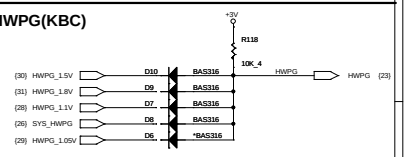
SM BUS PU(KBC)







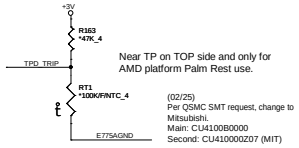
HWPG(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	APU
SM Bus 3	
SM Bus 4	

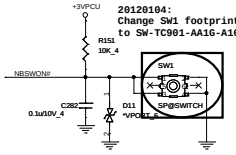
PALM REST THERMAL SENSOR (THM)



Near TP on TOP side and only for AMD platform Palm Rest use.

(02/25)
Per QSMC SMT request, change to Mitsubishi.
Main: CU4100B0000
Second: CU410000Z07 (MIT)

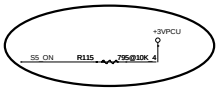
POWER-ON SWITCH (KBC)



20120104:
Change SW1 footprint from sw-tc017-ps11bt-6p-smt
to SW-TC901-AA1G-A160T-6P

20120217:
Change SW1 footprint from DHP00AC1G01 to DHP00532W00

Ramp 0221:
chage SW1 P/N from DHP00AC1G01 to DHP00533B00



Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	EC NPCE795CA0DX	1A

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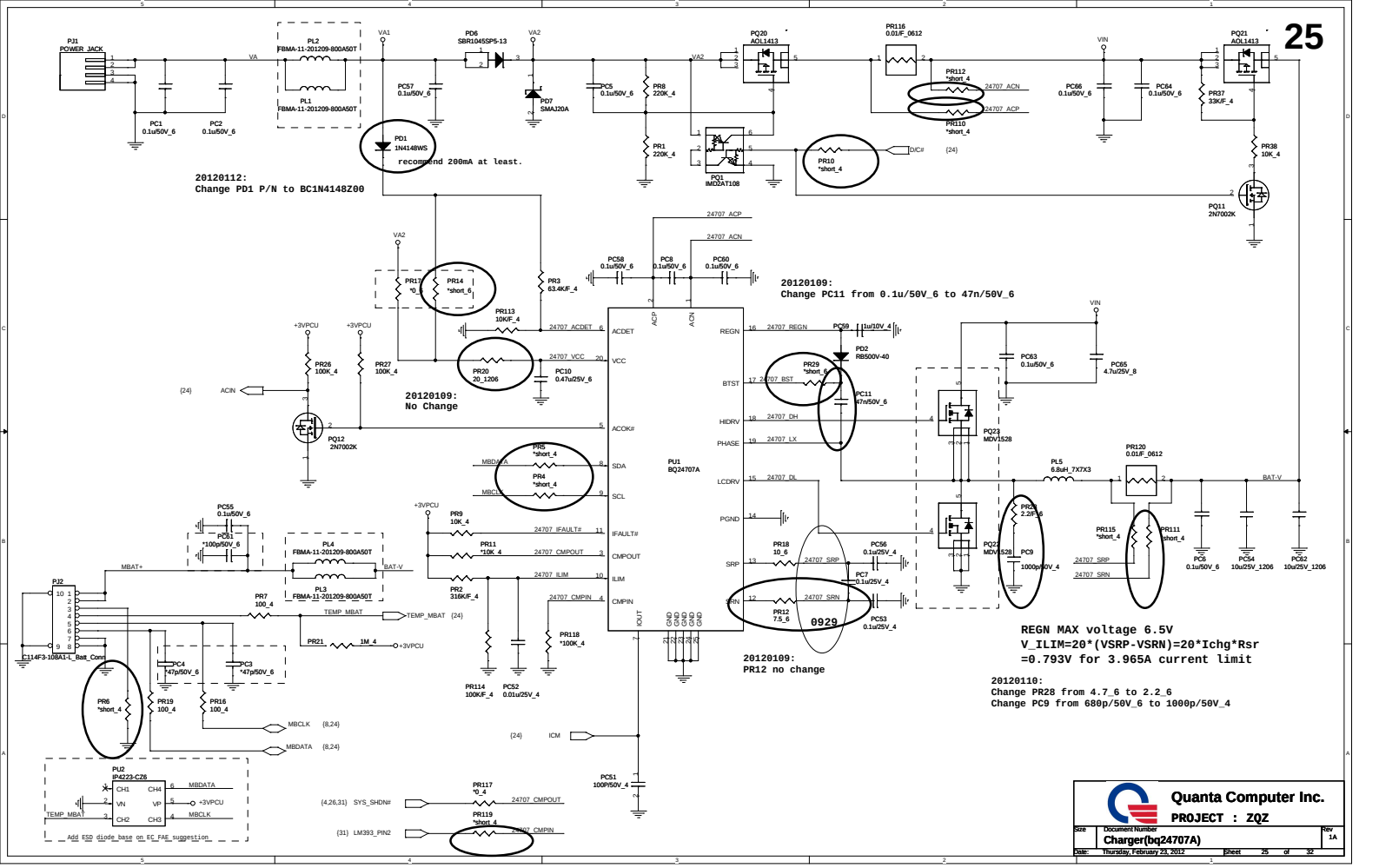

Quanta Computer Inc.
PROJECT : ZQZ

Size	Document Number	Rev
	Charger(bq24707A)	1A
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MAIND → MAIND (28,30,31)

SYS_SHDN# → SYS_SHDN# (4,25,31)

Ven=7.23V

111220: Change +3VPCU_SRC name to VL

(24) SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 5A
PEAK : 6.6A
OCP : 8A
Width : 200mil

20111226:
Change PC73 value from 0.1u_6 to 2200p_4

+3VPCU
3.3Volt +/- 5%
TDC : 5.02A
PEAK : 6.3A
OCP : 7.5A
Width : 200mil

20111226:
Change PC90 value from 0.1u_6 to 2200p_4

PU4 RT8223PZQW

20120113:
Change PC104 P/N from CC73301MZB2 to CC73301MZ00

OCP:8A
L(ripple current) =(9-5)*5/(2.2u*0.4M*9) =2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA =94.32K

20120106:
Remove PR74

OCP:7.5A
L(ripple current) =(9-3.3)*3.3/(2.2u*0.5M*9) ~1.9A
Iocp=7.5-(1.9/2)=6.55A
Vth=6.55A*14mOhm=91.7mV
R(Ilim)=(91.7mV*10)/10uA ~91K

20120113:
Change PC101 P/N from CC73301MZB2 to CC73301MZ00

20120110:
Change PR153 from 4.7_6 to 2.2_6
Change PC93 from 680p/50V_6 to 1000p/50V_4

+5V_S5
TDC : 1.88A
PEAK : 2.5A
Width : 80mil

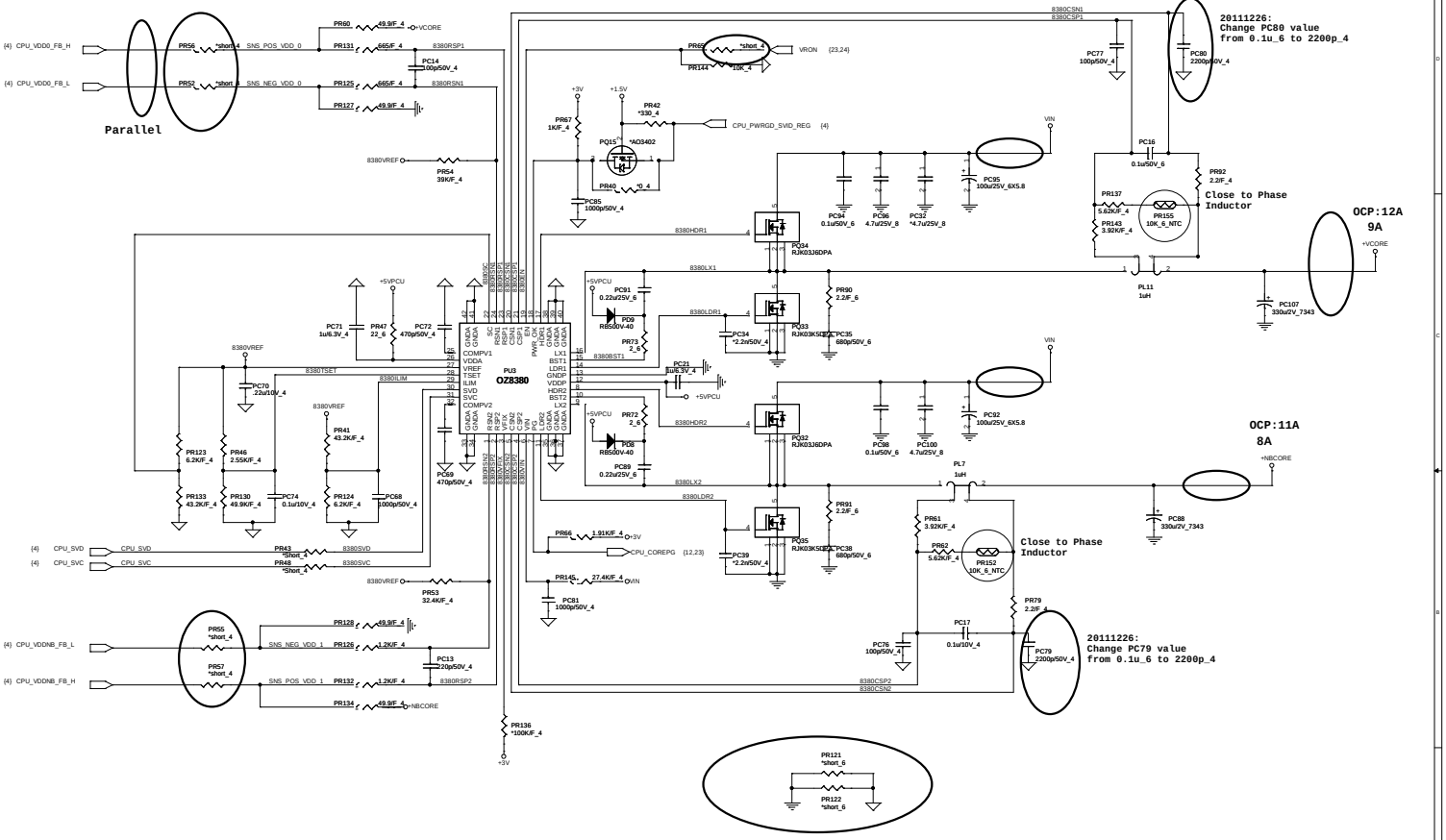
+5V
TDC : 3.08A
PEAK : 4.1A
Width : 120mil

+3V
TDC : 2.48A
PEAK : 3.3A
Width : 100mil

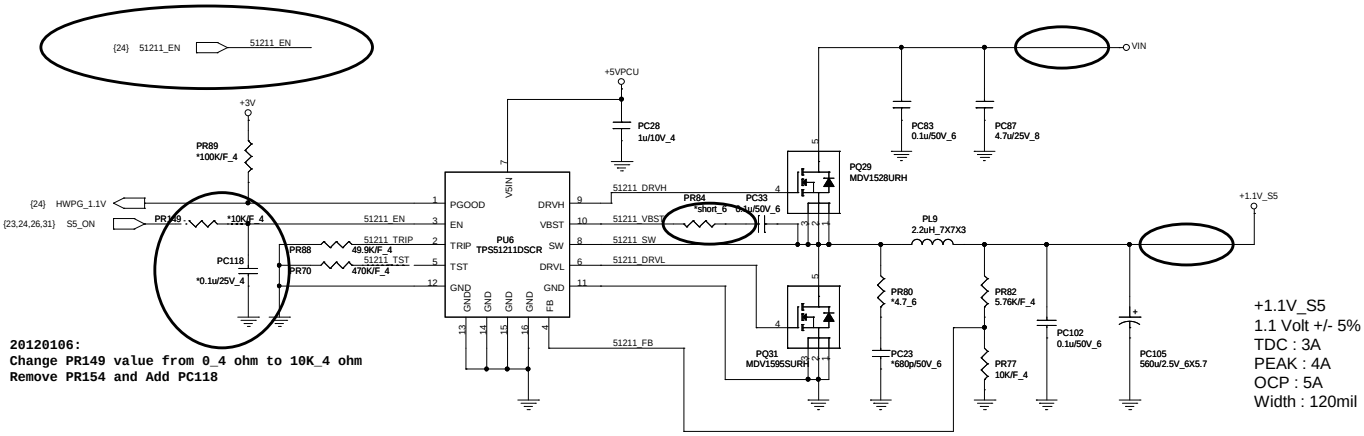
+3V_S5
TDC : 0.62A
PEAK : 0.84A
Width : 40mil

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date: Thursday, February 23, 2012	Sheet 26 of 32	


Parallel
OZ8380
20111226:
Change PC80 value
from 0.1u_6 to 2200p_4
Close to Phase
Inductor
OCP:12A
9A
OCP:11A
8A
Close to Phase
Inductor
20111226:
Change PC79 value
from 0.1u_6 to 2200p_4

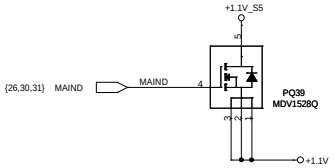
20120106:
Add net +1.1V_S5_EN to EC and add R452



20120106:
Change PR149 value from 0_4 ohm to 10K_4 ohm
Remove PR154 and Add PC118

+1.1V_S5
1.1 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil

OCP=5A
L ripple current
=(19-1.1)*1.1/(2.2u*290k*19)
=1.624A
Vtrip=5-(1.624/2)*14mohm
=0.058629V
Rlimit=0.058629/10uA*8=46.9Kohm



+1.1V
TDC : 2.73A
PEAK : 3.64A
Width : 120mil

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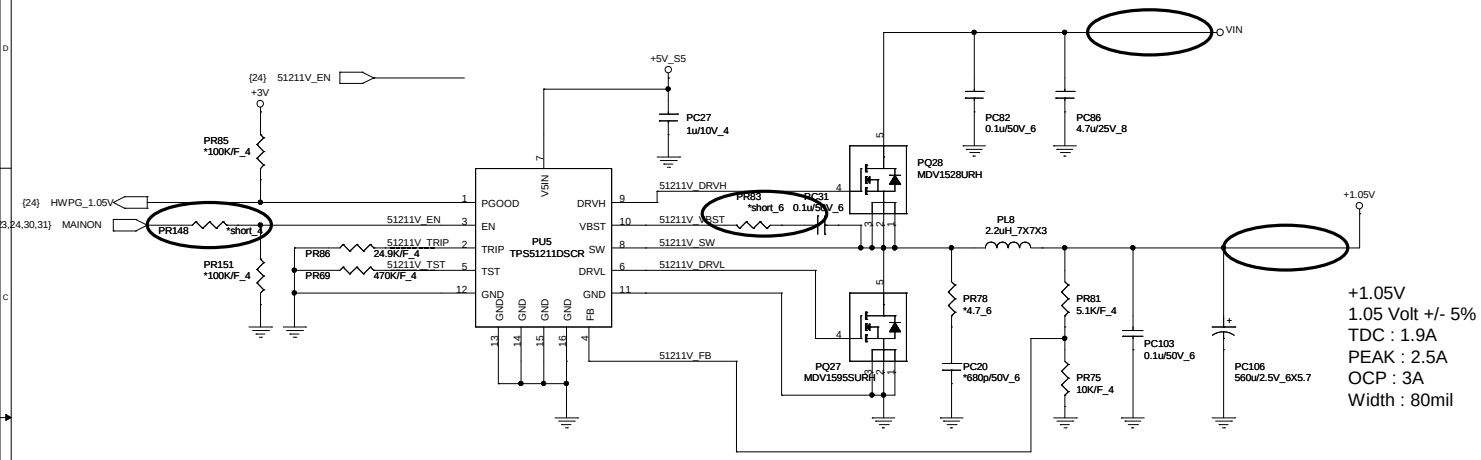

+1.05V
1.05 Volt +/- 5%
TDC : 1.9A
PEAK : 2.5A
OCP : 3A
Width : 80mil

OCP=3A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=3-(1.555/2)*14mohm
=0.03111V
Rlimit=0.03111/10uA*8=24.89Kohm

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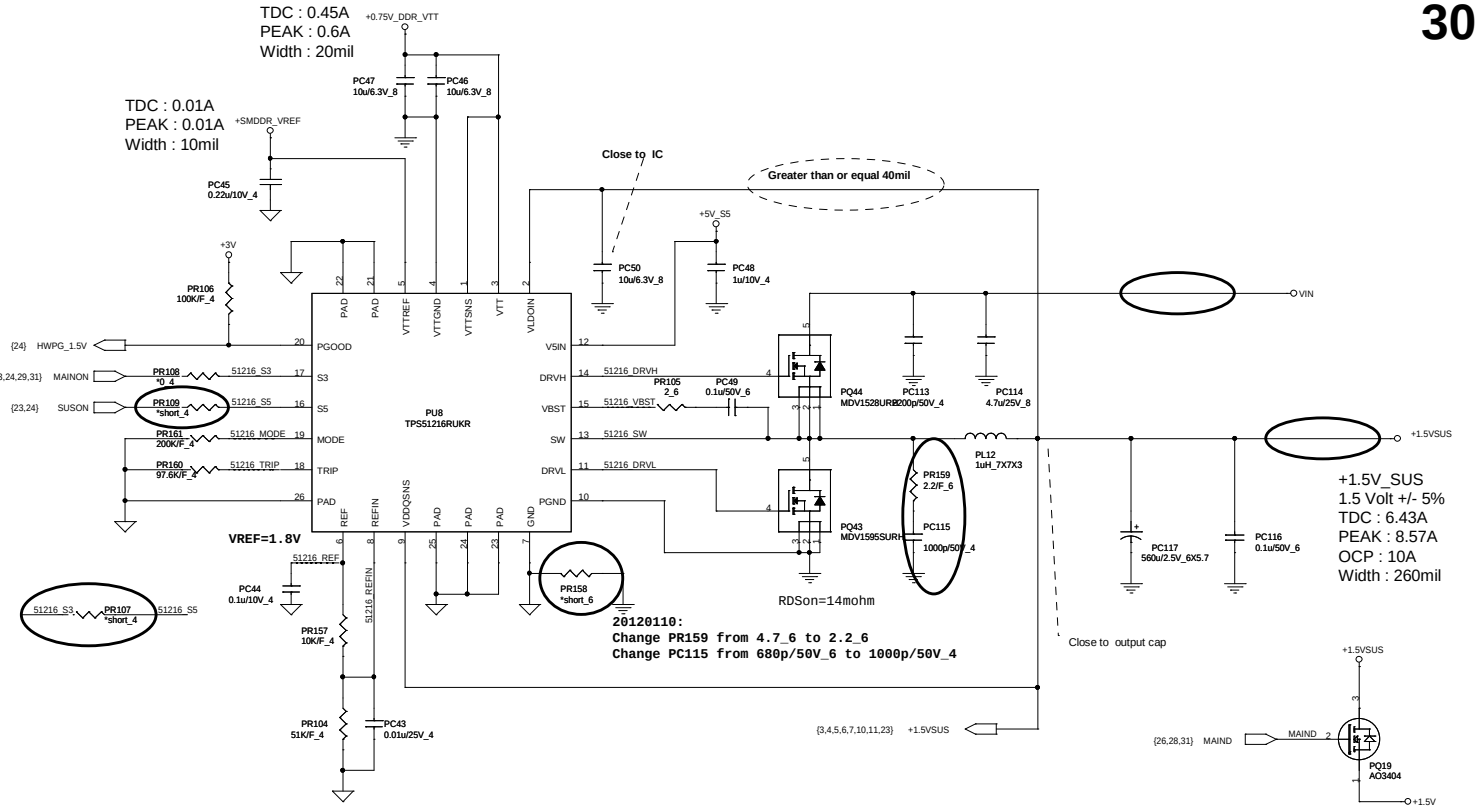

OCP=10A
L ripple current
=(19-1.5)*1.5/(1u*400k*19)
=3.454A
Vtrip=10-(3.454/2)*14mohm
=0.1158V
Rlimit=0.1158/10uA*8=92.657Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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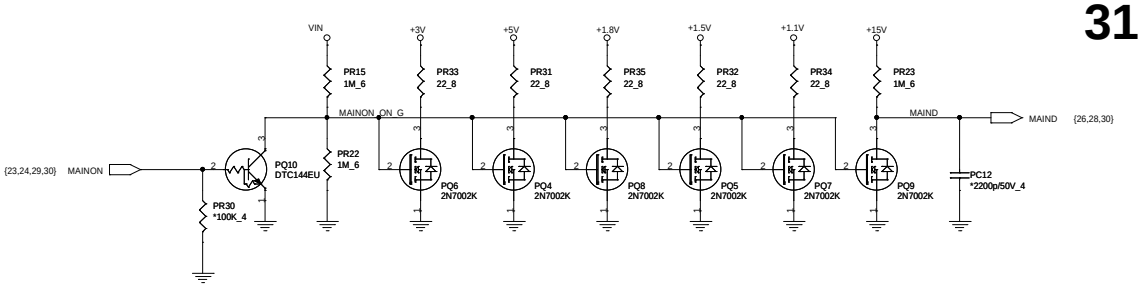
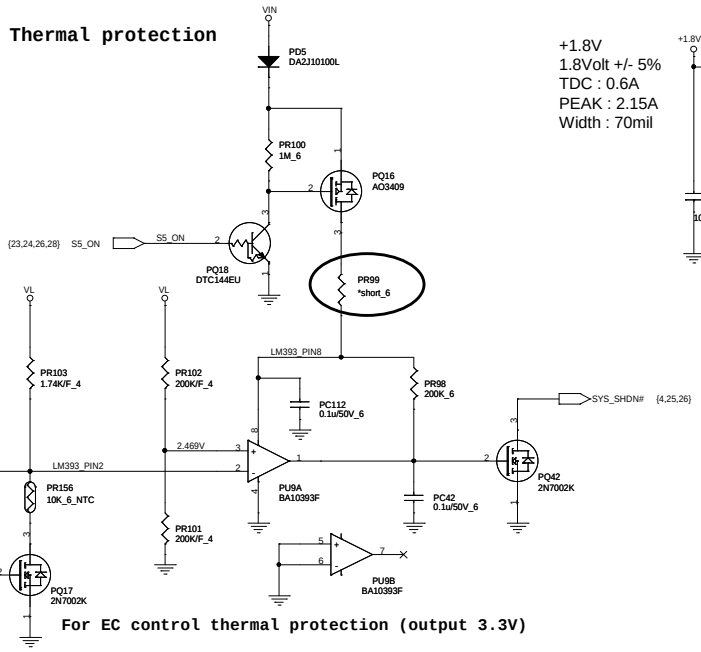
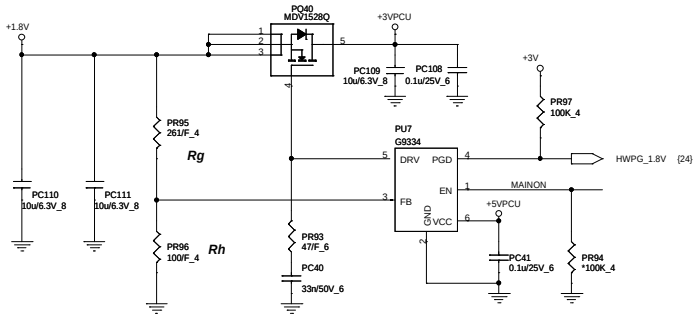


Thermal protection



For EC control thermal protection (output 3.3V)

+1.8V
1.8Volt +/- 5%
TDC : 0.6A
PEAK : 2.15A
Width : 70mil



*Vout1 = (1+Rg/Rh)*0.5*

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CHANGE LIST

Model ZQE/G M/B BOARD

MODEL	REV		Page	From	To
ZQZ M/B	A	First Release	1	1A	3A
			2	1A	3A
			3	1A	3A
	B	111220: page26--Change PR44 net from +3VPCU_SRC name to VL	4	1A	3A
		111220: Change all TP footprint to TP2650	5	1A	3A
		111226: page25--Change PR20 value from 20_1206ohm to 22_8ohm	6	1A	3A
		Change PR12 value from 7.5ohm to 10ohm	7	1A	3A
		page26&27--Change PC73, PC79, PC80, PC90 value from 0.1u_6 to 2200p_4	8	1A	3A
		111228: page20--Add R447, R448, Q26, Q27	9	1A	3A
		111230: page23--Swap PDAT_SMB and PCLK_SMB	10	1A	3A
		120103: page24--Change TP26 from U4.105 to U4.22	11	1A	3A
		Change net CPUFAN# from U4.22 to U4.105	12	1A	3A
		120104: Change PQ22,PQ23,PQ24,PQ25,PQ26,PQ27,PQ28,PQ29,PQ30,PQ31,PQ36,PQ38,,PQ39,	13	1A	3A
		PQ40,PQ43,PQ44 footprint to wdfn5-3_05x3_05-65	14	1A	3A
		120104: page13--Swap INT_EDIDCLK from CN1.32 to CN1.33	15	1A	3A
		Swap INT_EDIDDATA from CN1.33 to CN1.32	16	1A	3A
		Change SW1, SW2, SW3 footprint from sw-tc017-ps11bt-6p-smt to SW-TC901-AA1G-A160T-6P	17	1A	3A
		R30, R28, Q2, Q3 unstuff, R21 stuff	18	1A	3A
		page10--Add R449, R450, R451	19	1A	3A
		Add net N30960722	20	1A	3A
		120106: page26--Remove PR74	21	1A	3A
		page24--Remove net POWERSMAR_SW and add TP97	22	1A	3A
		page24--Remove net POWERSMARTLED and add TP95	23	1A	3A
		page24--Remove net +0.75V_ON and add TP96	24	1A	3A
		page28--Change PR149 value from 0_4 ohm to 422K_4 ohm	25	1A	3A
		page28--Remove PR154 and Add PC118	26	1A	3A
		page28--Add net +1.1V_S5_EN to EC and add R452	27	1A	3A
		page24--Connect net SML1ALERT# to EC and add R453	28	1A	3A
		120109: page26--Change C27 and C31 from10P_4 to 15p_4	29	1A	3A
		120109: page25--PR20 No change	30	1A	3A
		120109: page25--Change PC11 from 0.1u/50V_6 to 47n/50V_6	31	1A	3A
		120109: page25--PR12 no Change	32	1A	3A
		120109:Remove JP9, JP3, JP12, JP3, JP10, JP11, JP13, JP14, JP7, JP1, JP2, JP4, JP5, JP6	33	1A	3A
		120110:page25--Change PR28 from 4.7_6 to 2.2_6, Change PC9 from 680p/50V_6 to 1000p/50V_4	34	1A	3A
		120110:page26--Change PR153 from 4.7_6 to 2.2_6, Change PC93 from 680p/50V_6 to 1000p/50V_4	35	1A	3A
		120110:page30--Change PR159 from 4.7_6 to 2.2_6, Change PC115 from 680p/50V_6 to 1000p/50V_4	36	1A	3A
		120110:page13--Change L14, L17, L23 from BLM18BA470SN1_6 to BLM18BB750SN1D	37	1A	3A
		120110:page13--Change C398 from .1u_10V_4 to 1000p/50V_4	38	1A	3A
		120110:page9--Change R364 from 22_4 to 33_4 -->for slewrate issue	39	1A	3A
		120111:page16--modify surge solution and change D14 P/N from CY003100Z06 to CY231T20Z00	40	1A	3A
		120111:page10--Connect R451 net from FCH_SPI_CS0# to SPI_CS	41	1A	3A
		120111:page14--Add C517 for hdmi detect issue	42	1A	3A
		120111:page16--Change R196 footprint to 0805	43	1A	3A
		120112:page09--Change R359 from 22_4 to 33_4-->follow vender suggestion	44	1A	3A
		120112:page24--Change R110, R112, R116, R114 from 10k to 4.7k-->follow vender suggestion	45	1A	3A
		120112:Change PQ24, PQ26, PQ28, PQ29, PQ44 P/N from BAM74100001 to BAM15280000	46	1A	3A
		120112:Change PQ25, PQ27, PQ30, PQ31, PQ43 P/N from BAM77020000 to BAM15950000	47	1A	3A
		120112:Change PQ32, PQ34 P/N from BAM14480000 to BAM03J60000	48	1A	3A
		120112:Change PQ33, PQ35 P/N from BAM17180000 to BAM03K50000	49	1A	3A
		120113:page25--Change PD1 P/N to BC1N4148Z00	50	1A	3A
		120113:page16--Change Change L31 P/N from CX08T601010 to CX8AG601003	51	1A	3A
		120113:page26--Change PC101, PC104 P/N from CC73301MZB2 to CC73301MZ00	52	1A	3A
		120217:page22--Change R180, R182 from 255 to 590ohm	53	1A	3A
		120217:page22--Change R1 from 100 to 80.6ohm	54	1A	3A
		120217:page23,24--Change SW1, SW2, SW3 from DHP00AC1G01 to DHP00532W00			
	C	120221:page21-C303 unstuff			
		120221:page21-BT component unstuff			
		120221:page22-Change R185 from422 to 255ohm			
		120221:page24-chage SW1 P/N from DHP00AC1G01 to DHP00533B00			
		120221:page13-Remove L3			
		120221:page21-Remove L27, RP5, RP6, L26, L30, L28			
		120221:page17-Add IOAC circuit, R454, Q28, C518, R455,U23, R456, R457,, R460			
		Add Net WLAN_OFF, WLAN_OFF_R, IOAC_LANPWR#, PLTRST#_R, IOAC_RST#			
		120221:page24-Add R458, Add net PLTRST#_C			
		120221:page18-Add R459			
		120223:page9-Remove RP3,RP4, AddR461, R462, R463, R464			
		120223:page14-Change R88, R94, R103, R109 value from 100 to 120ohm and stuff			
		120223:page17-Add Q29, Q30, Add net PCIE_REQ_WLAN#_R, PCIE_WAKE#_WLAN_R			

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ZQZ	PCBA NO.	REV:	DOC. NO :	
APPROVED BY : Spruce Wu	CHECK BY :Martin Tsai	DRAWING BY : Allen Hsu	DATE :	SHEET 1